

CMOS Matrix-Vector Multiplier

ECE 533 – Final Design Review

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Outline Review

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \cdot \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} ax + by \\ cx + dy \end{bmatrix}$$

Input:

- $a, b, c, d, x, y \rightarrow$ 4-bit unsigned each

Product:

- $ax, by, cx, dy \rightarrow$ 8-bit unsigned each

Output:

- $(ax + by), (cx + dy) \rightarrow$ 9-bit unsigned

What we need:

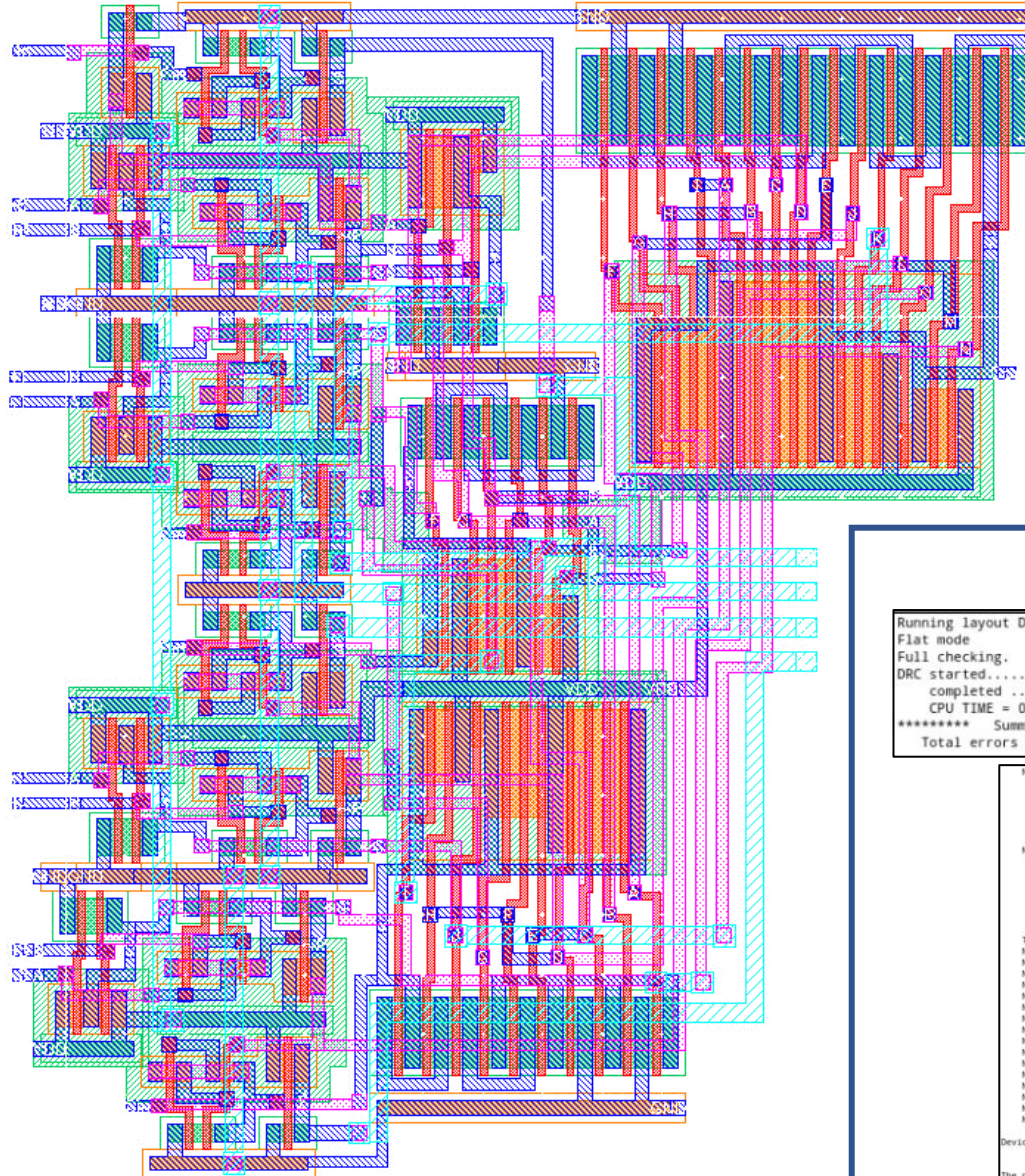
- 4×4 Multiplier
- 8-bit Adder
- Bank of D-Latch

Adder Type:

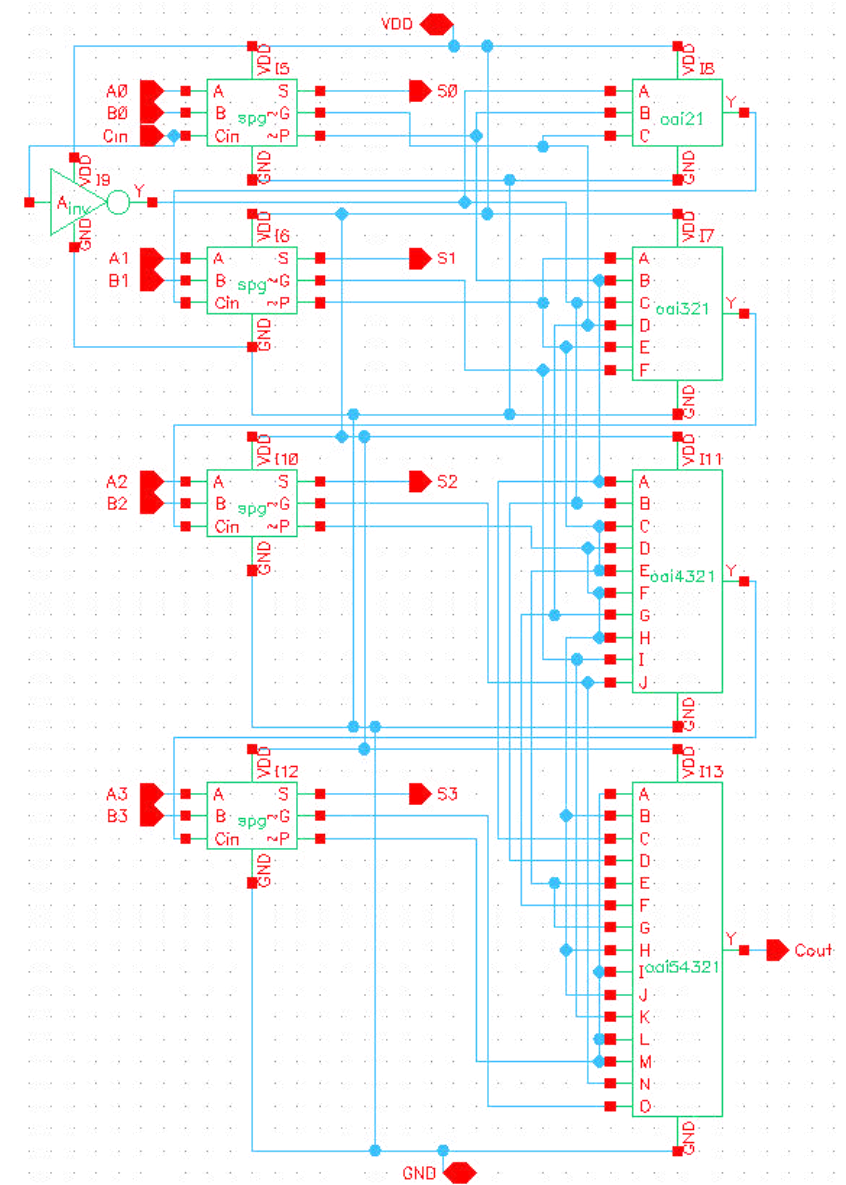
- Carry-lookahead Adder (CLA)

Where we left: 4-bit CLA unit

Layout



Schematic



DRC & LVS

Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Thu Nov 17 22:34:07 2022
completedThu Nov 17 22:34:07 2022
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "fa_test layout" *****
Total errors found: 0

Net-list summary for /home/salam2/ece533/cadence/LVS/layout/netlist
count
78 nets
16 terminals
67 pmos
67 nmos

Net-list summary for /home/salam2/ece533/cadence/LVS/schematic/netlist
count
78 nets
16 terminals
67 pmos
67 nmos

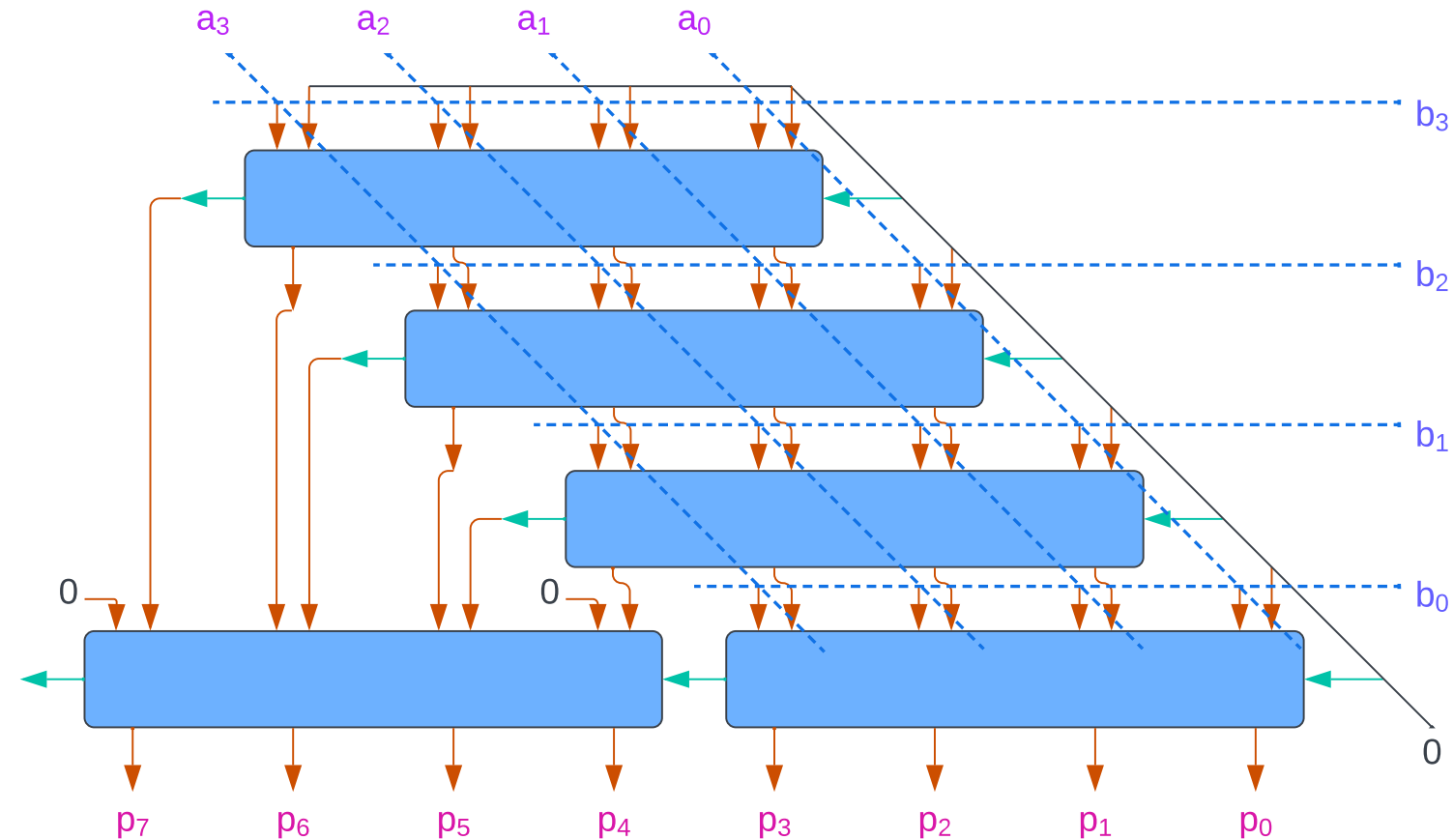
Terminal correspondence points

N68	N3	A0
N67	N6	A1
N66	N11	A2
N65	N26	A3
N76	N2	B0
N75	N5	B1
N74	N24	B2
N72	N27	B3
N70	N4	Cin
N71	N15	Cout
N69	N1	GND
N64	N9	S0
N63	N10	S1
N62	N13	S2
N77	N25	S3
N73	N8	VDD

Devices in the netlist but not in the rules:
pmos nmos

The net-lists match.

4x4 Multiplier

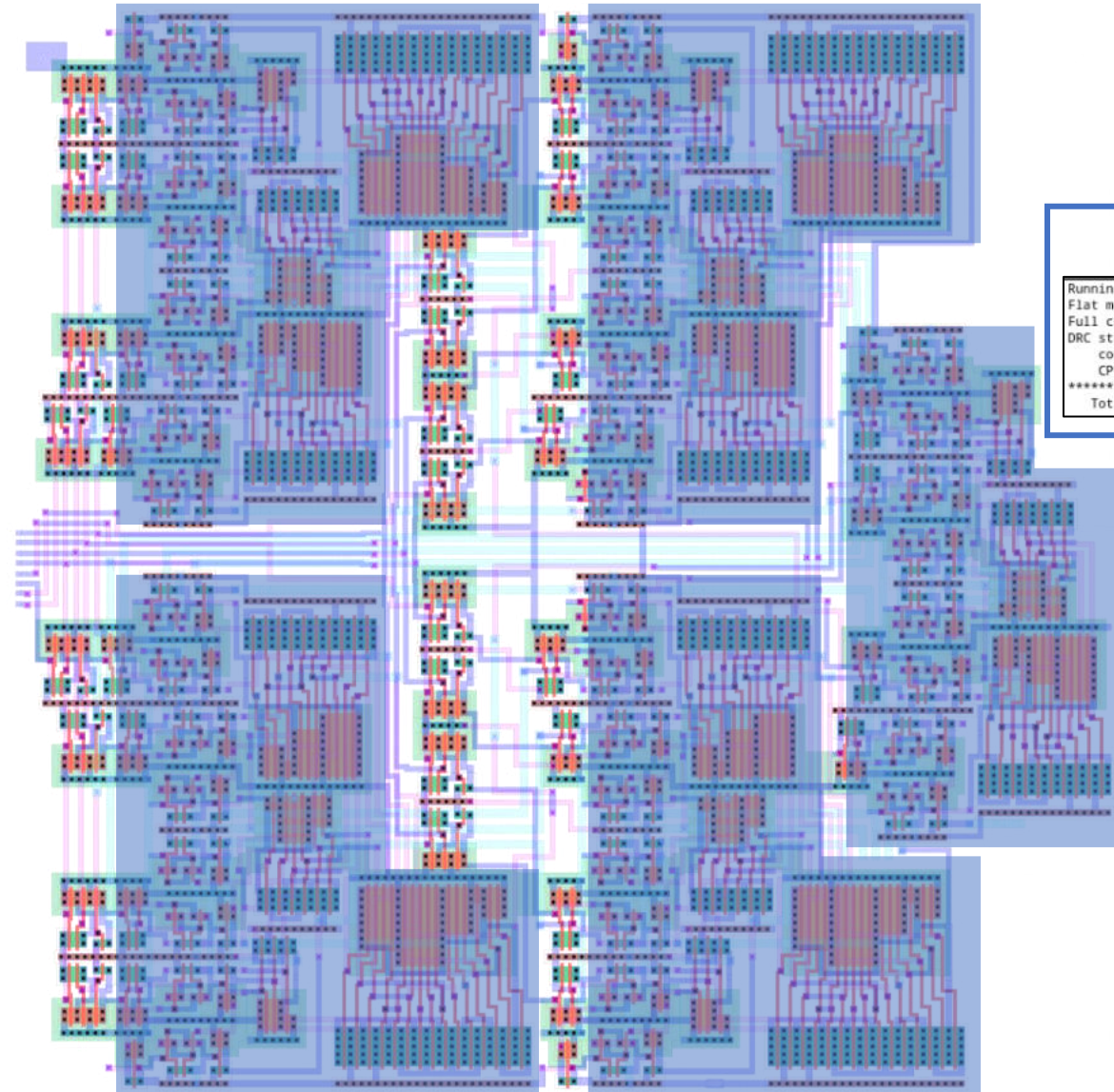


Things to consider:

- We need
 - 5 units of CLA4
 - 16 units of AND2.
- C_{out} of last CLA4 is unnecessary.
 - Remove OAI54321 (30 T) from that.
- P7 will be slowest (obviously).

continued...

Layout



DRC & LVS

```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Thu Dec 1 22:38:49 2022
completed ....Thu Dec 1 22:38:50 2022
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "multi4 layout" *****
Total errors found: 0
```

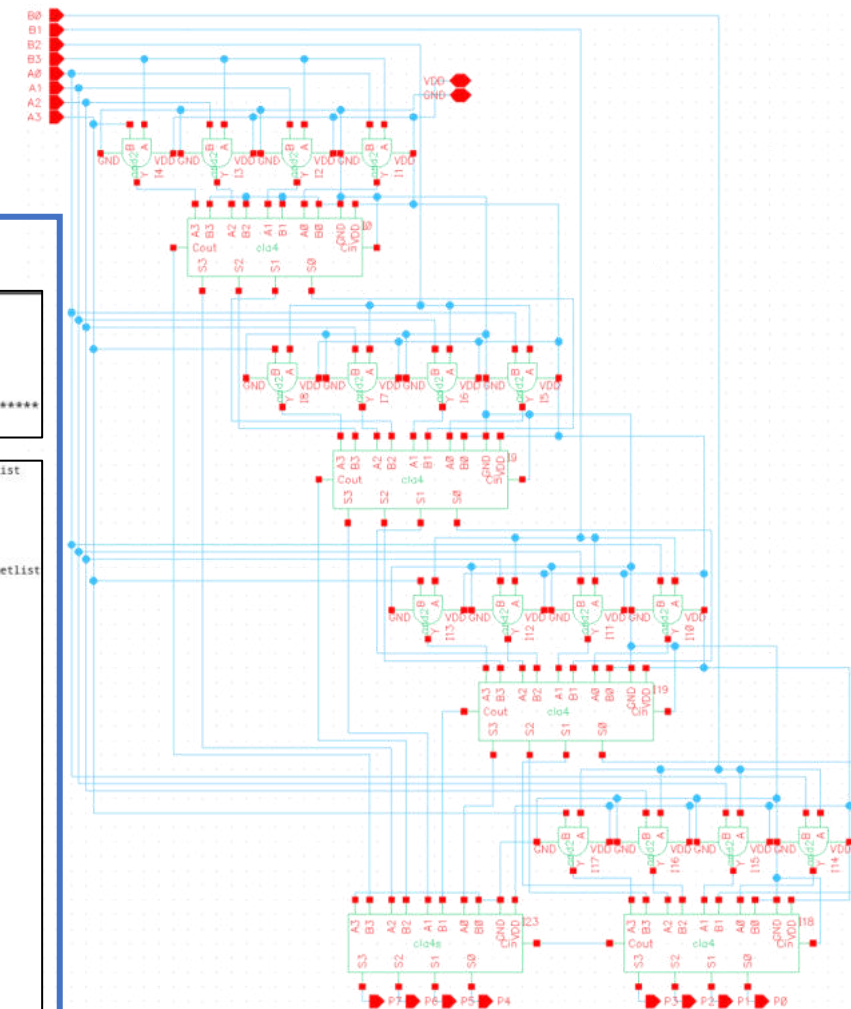
```
Net-list summary for /home/salam12/ece533/cadence/LVS/layout/netlist
count
378      nets
18       terminals
368      pmos
368      nmos

Net-list summary for /home/salam12/ece533/cadence/LVS/schematic/netlist
count
378      nets
18       terminals
368      pmos
368      nmos
```

```
Terminal correspondence points
N363    N3      A0
N362    N2      A1
N361    N1      A2
N360    N0      A3
N377    N49     B0
N376    N48     B1
N375    N47     B2
N373    N46     B3
N364    N12     GND
N372    N44     P0
N371    N40     P1
N370    N35     P2
N369    N33     P3
N368    N32     P4
N367    N43     P5
N366    N45     P6
N365    N34     P7
N374    N18     VDD
```

```
Devices in the netlist but not in the rules:
pmos nmos
The net-lists match.
```

Schematic

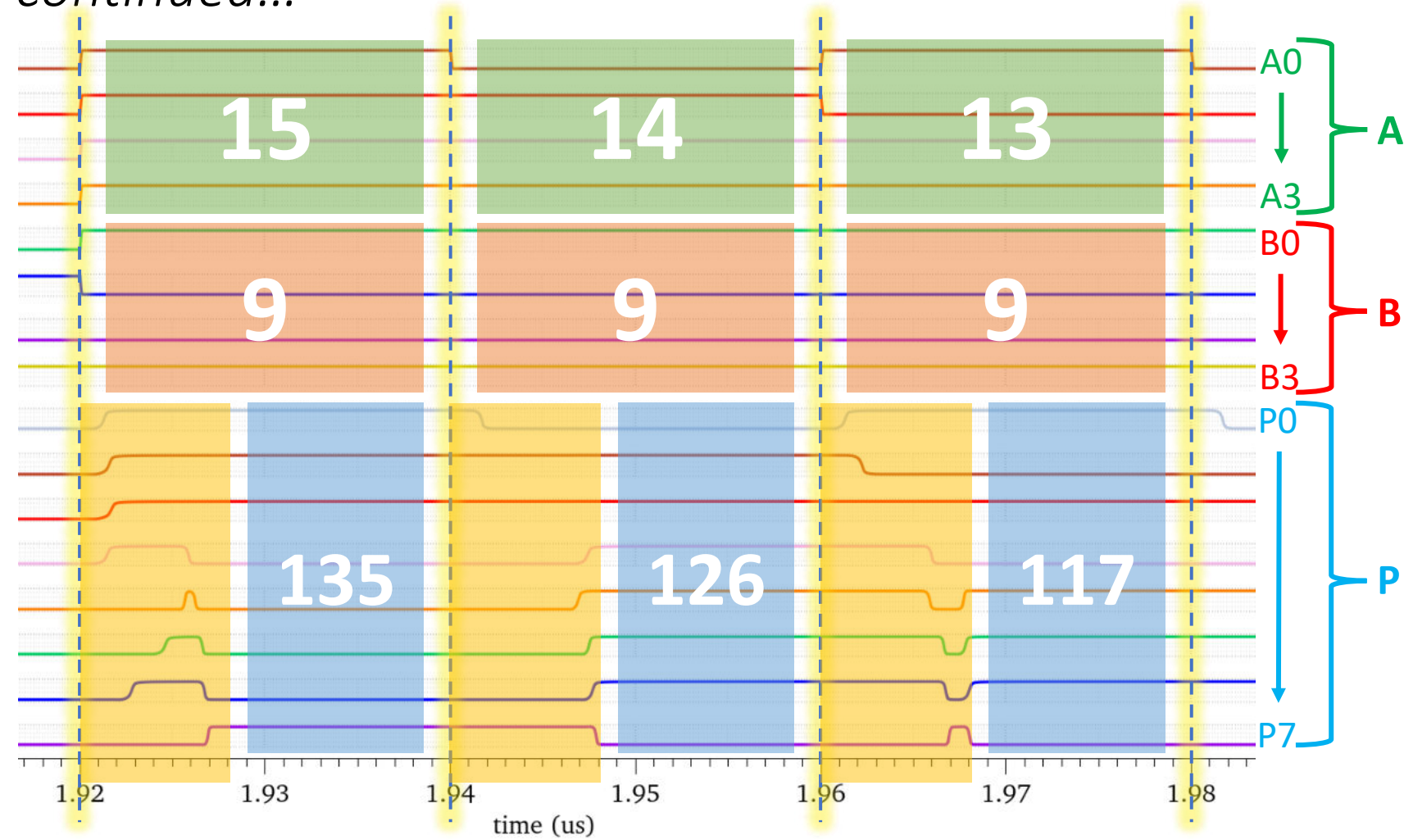


4x4 Multiplier Transient Analysis (*cropped*)



* We don't need C_{out} of last CLA4.

continued...

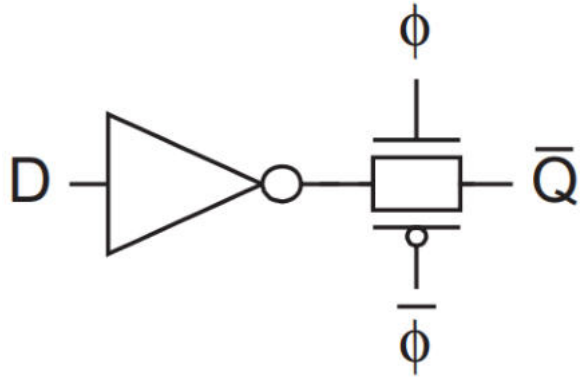


Note:

- Inputs are changing at 25 MHz here.
 - could be increased up to 50 MHz
- t_{pd} is 8 ns → will affect next stage

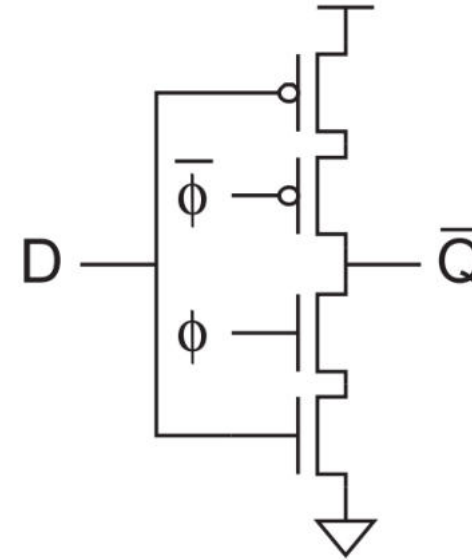
Dynamic D-Latch

Transmission Gate based



- ✓ Slightly faster:
 - Both FETs work in parallel

Clocked CMOS (C²MOS)



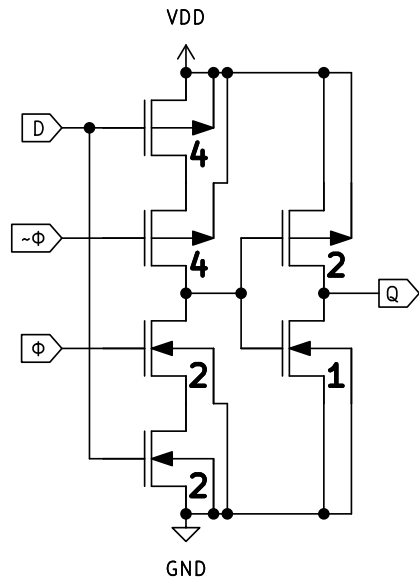
- ✓ Slightly smaller:
 - Eliminates 2 contacts

Problem with dynamic output:

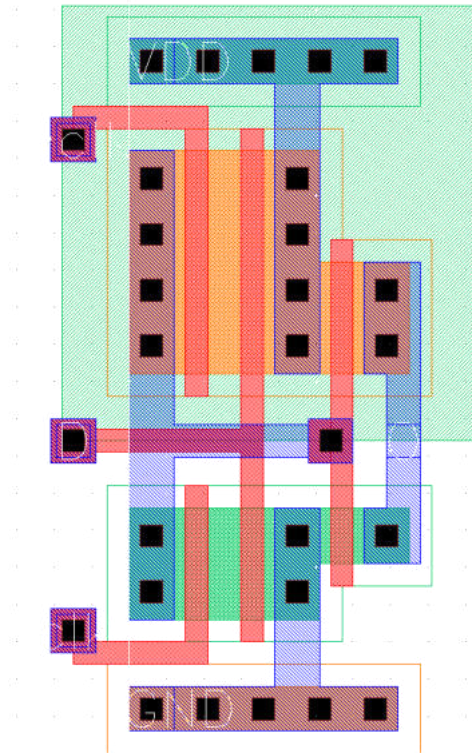
- May lose value due to subthreshold leakage
- May lose value during burn-in test

continued...

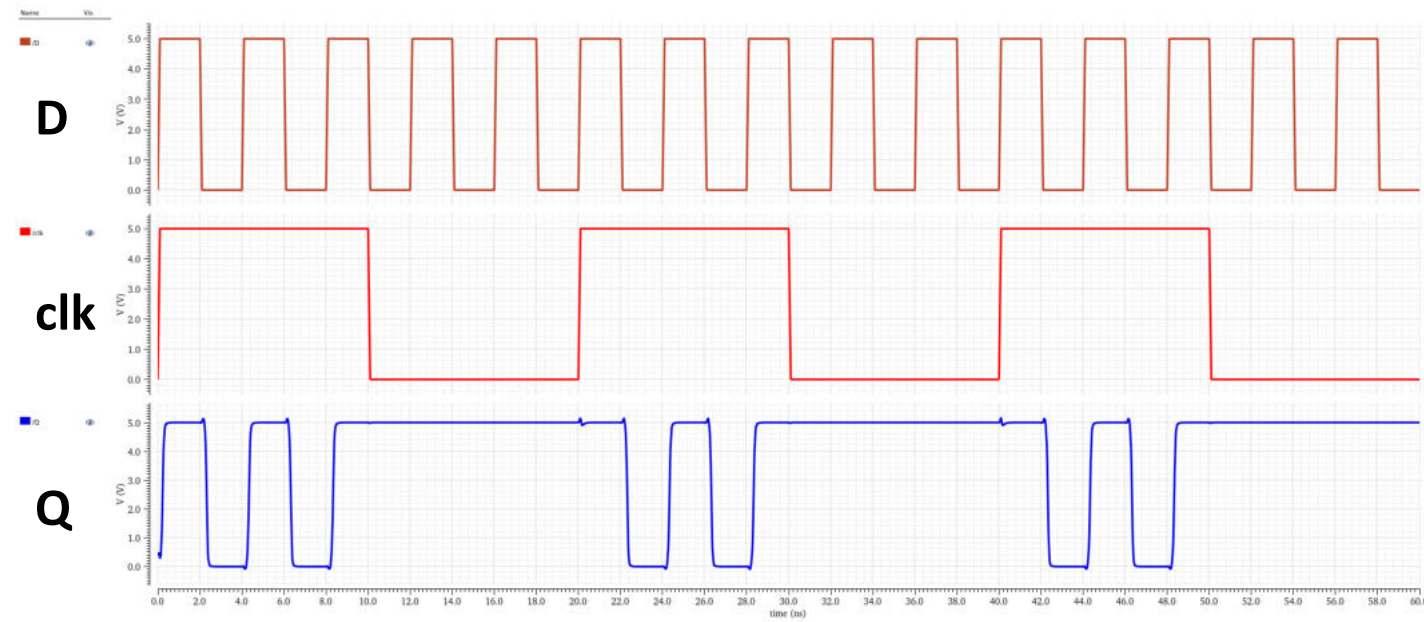
Schematic



Layout



C²MOS Latch Transient Analysis (*extracted*)



As expected,

- Q follows D while clk is true.
- Q holds Q_{old} while clk is false.

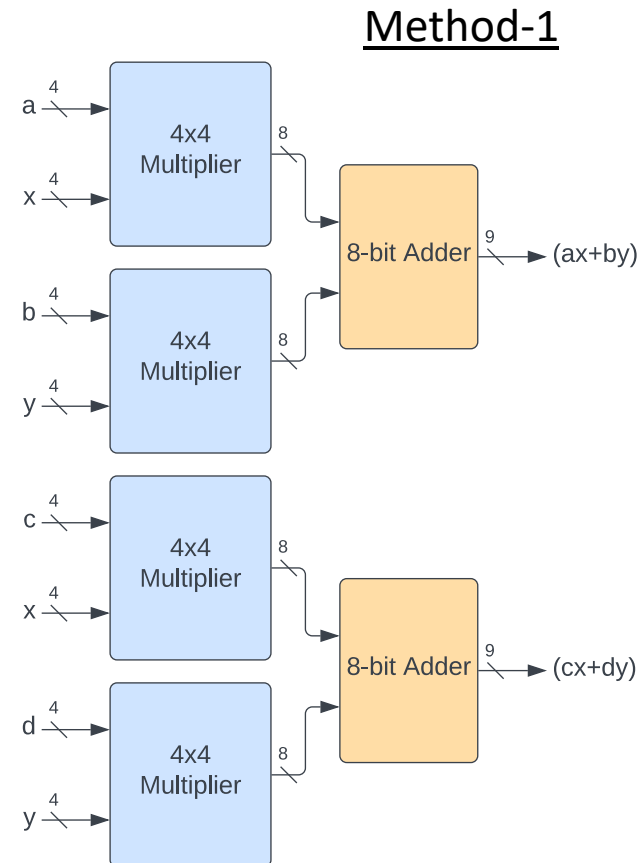
But,

- t_{pdq} is not bad, but not good either.

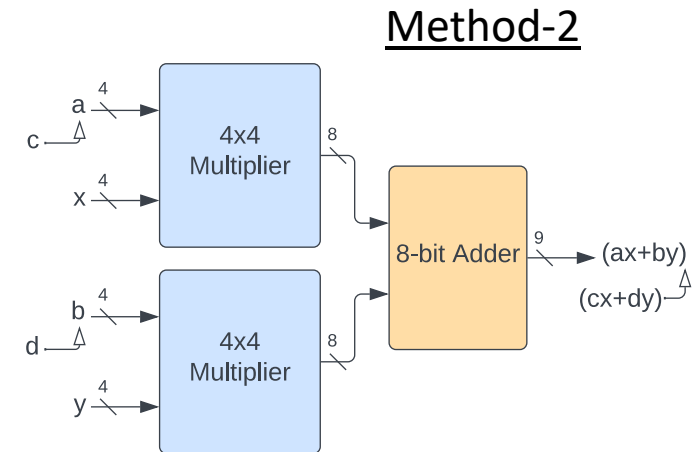
Possible Methods of Final Design

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \cdot \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} ax + by \\ cx + dy \end{bmatrix}$$

Assume:
Inputs are driven from D-FF.
Outputs are sampled by D-FF.



- ✓ Fastest method (T_{clk})
 - Both outputs concurrently available after t_{pd}
 - Outputs ready to be sampled at next posedge of D-FF
- ✓ No internal clock needed
- ❖ Enormous area required

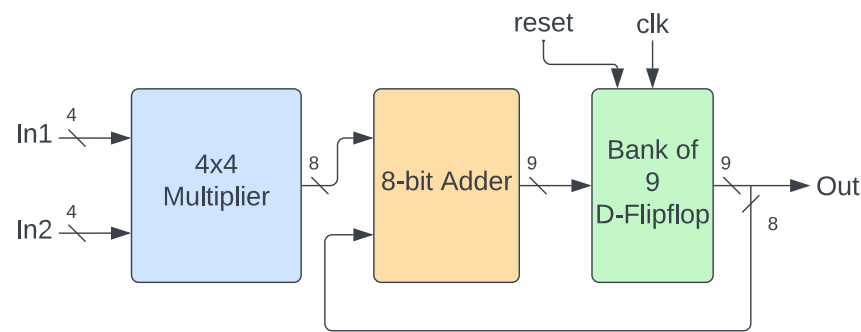


- ❖ Moderately fast method ($2 \times T_{clk}$)
 - Inputs are serially driven.
 - 2nd output ($cx + dy$) is sampled one T_{clk} after 1st output is sampled.
- ✓ No internal clock needed
- ❖ Huge area still required
 - even after 50% reduction

	Posedge		
	0	1	2
In1	a	c	
In2	x	x	
In3	b	d	
In4	y	y	
Out		$ax + by$	$cx + dy$

continued...

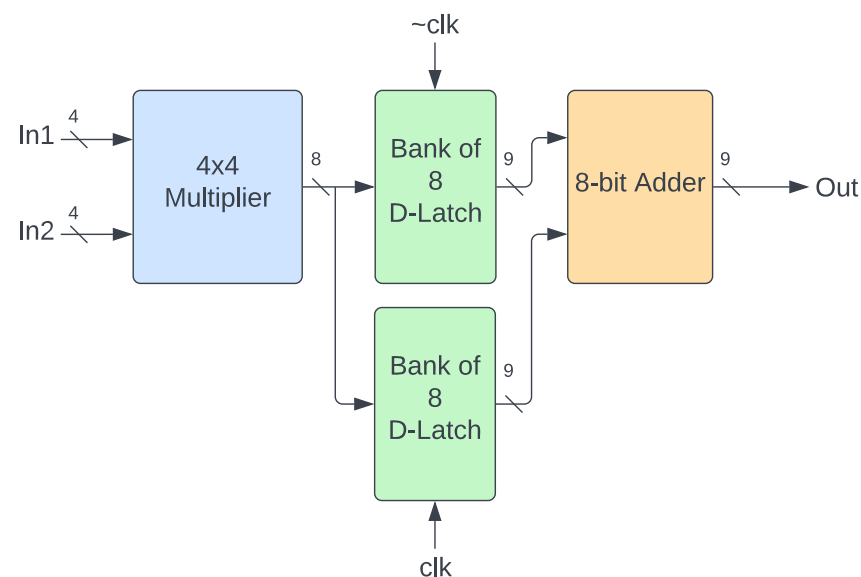
Method-3



- ❖ Slowest method ($4 \times T_{clk}$)
 - Inputs are serially driven.
- ❖ Internal clock needed
- ❖ Reset signal needed
 - Reset the D-FF bank at beginning, reset it again after $(ax + by)$ is sampled.
- ✓ Small area required

Posedge					
	0	1	2	3	4
In1	a	b	c	d	
In2	x	y	x	y	
Out		$ax + 0$	$ax + by$	$cx + 0$	$cx + dy$

Method-4

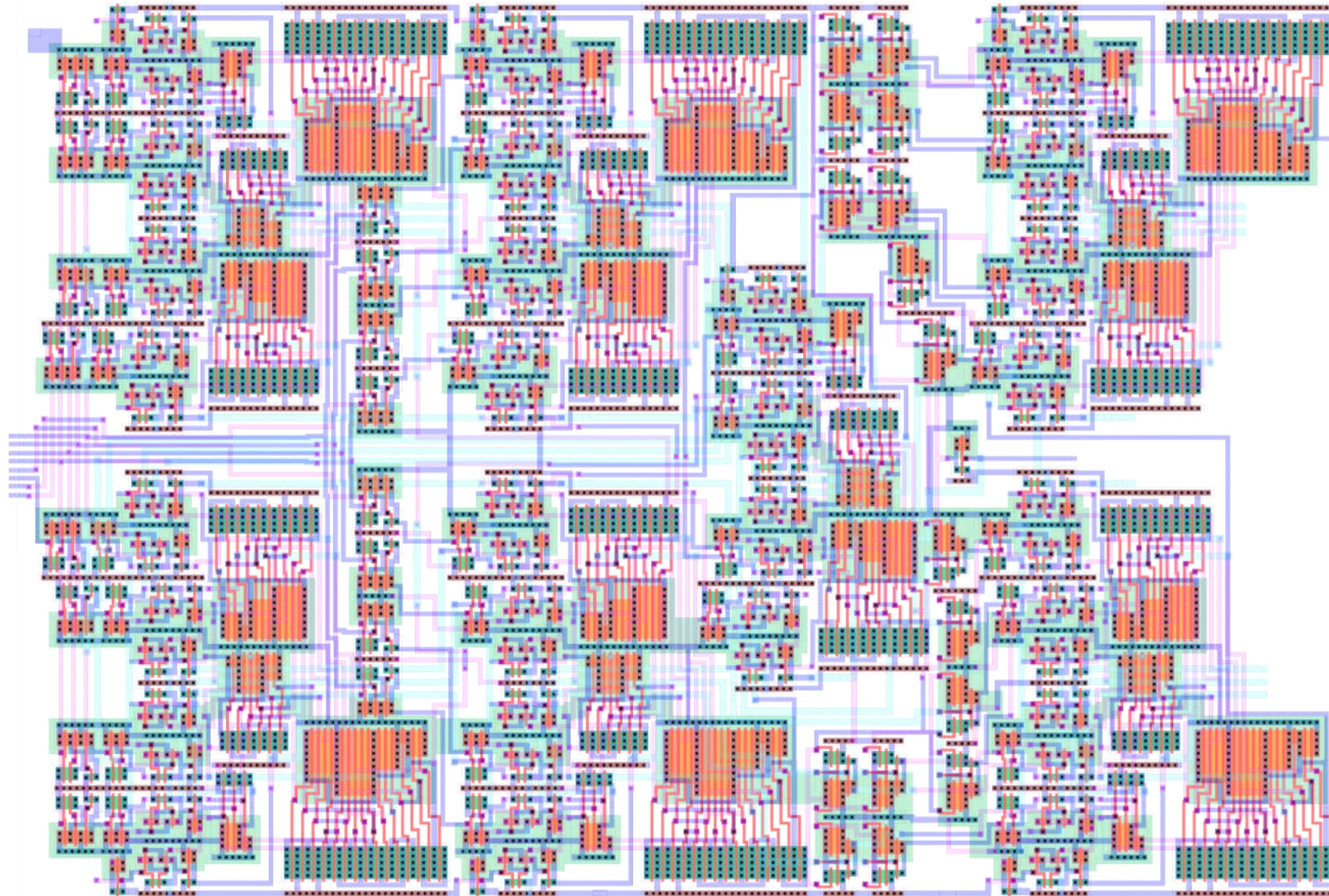


- ✓ Moderately fast method ($2 \times T_{clk}$)
 - TDM is employed for D-Latch banks.
- ❖ Internal clock needed
- ✓ Reset signal not needed
- ✓ Smallest area required

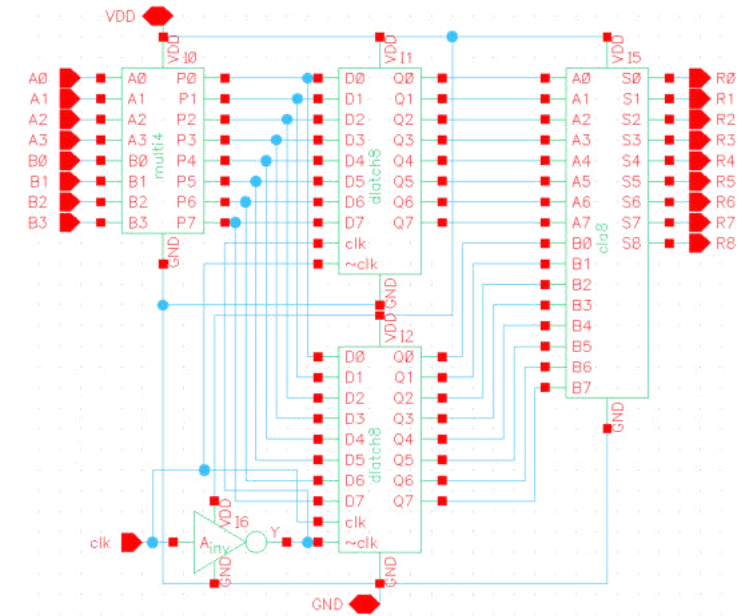
clk Level				
	1	0	1	0
In1	a	b	c	d
In2	x	y	x	y
Out	$ax + ?$	$ax + by$	$cx + by$	$cx + dy$

Full Design: Matrix-Vector Multiplier

Layout



Schematic



Net-list summary for /home/salam12/ece533/cadence/LVS/layout/netlist

count	nets
578	20
551	terminals
551	pmos
551	nmos

Net-list summary for /home/salam12/ece533/cadence/LVS/schematic/netlist

count	nets
578	20
551	terminals
551	pmos
551	nmos

Terminal correspondence points

Terminal	correspondence	points
N564	N14	A0
N562	N15	A1
N560	N35	A2
N558	N36	A3
N577	N37	B0
N576	N38	B1
N575	N39	B2
N573	N40	B3
N571	N17	GND
N570	N41	R0
N569	N42	R1
N568	N43	R2
N567	N0	R3
N566	N1	R4
N565	N2	R5
N563	N3	R6
N561	N4	R7
N559	N5	R8
N574	N16	VDD
N572	N44	clk

Devices in the netlist but not in the rules:
pmos nmos

The net-lists match.

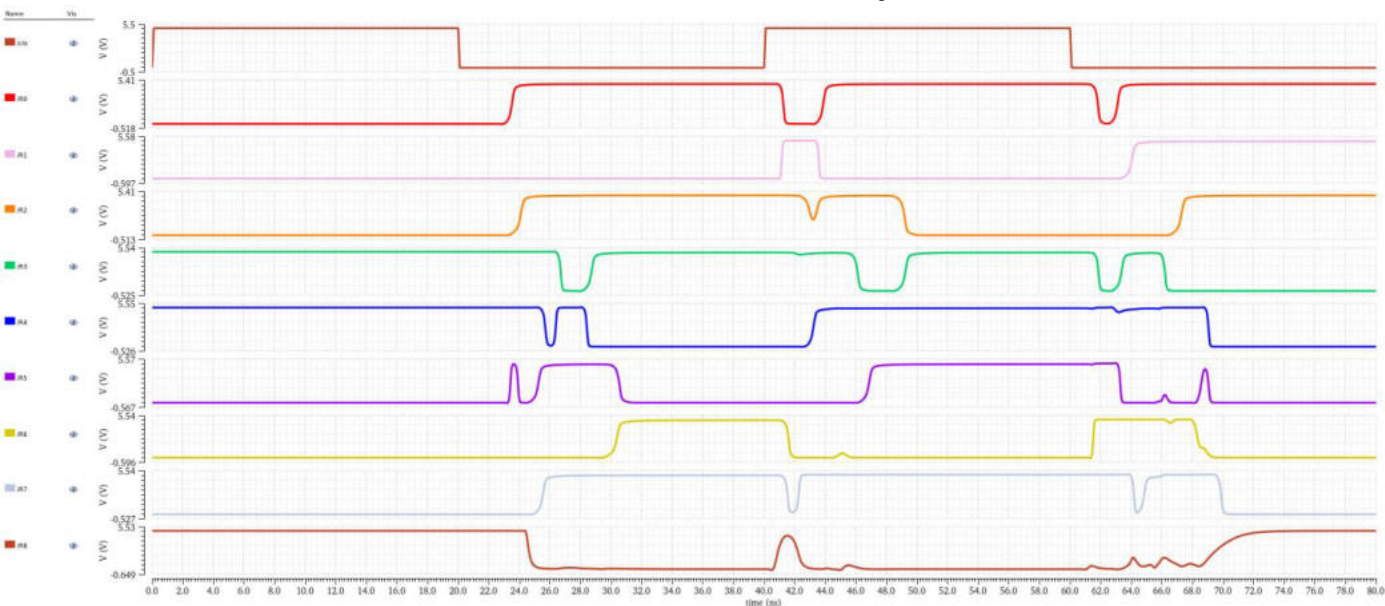
DRC

Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Dec 5 17:29:17 2022
completedMon Dec 5 17:29:18 2022
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "matvec layout"
Total errors found: 0

LVS

continued...

Transient Analysis



Schematic

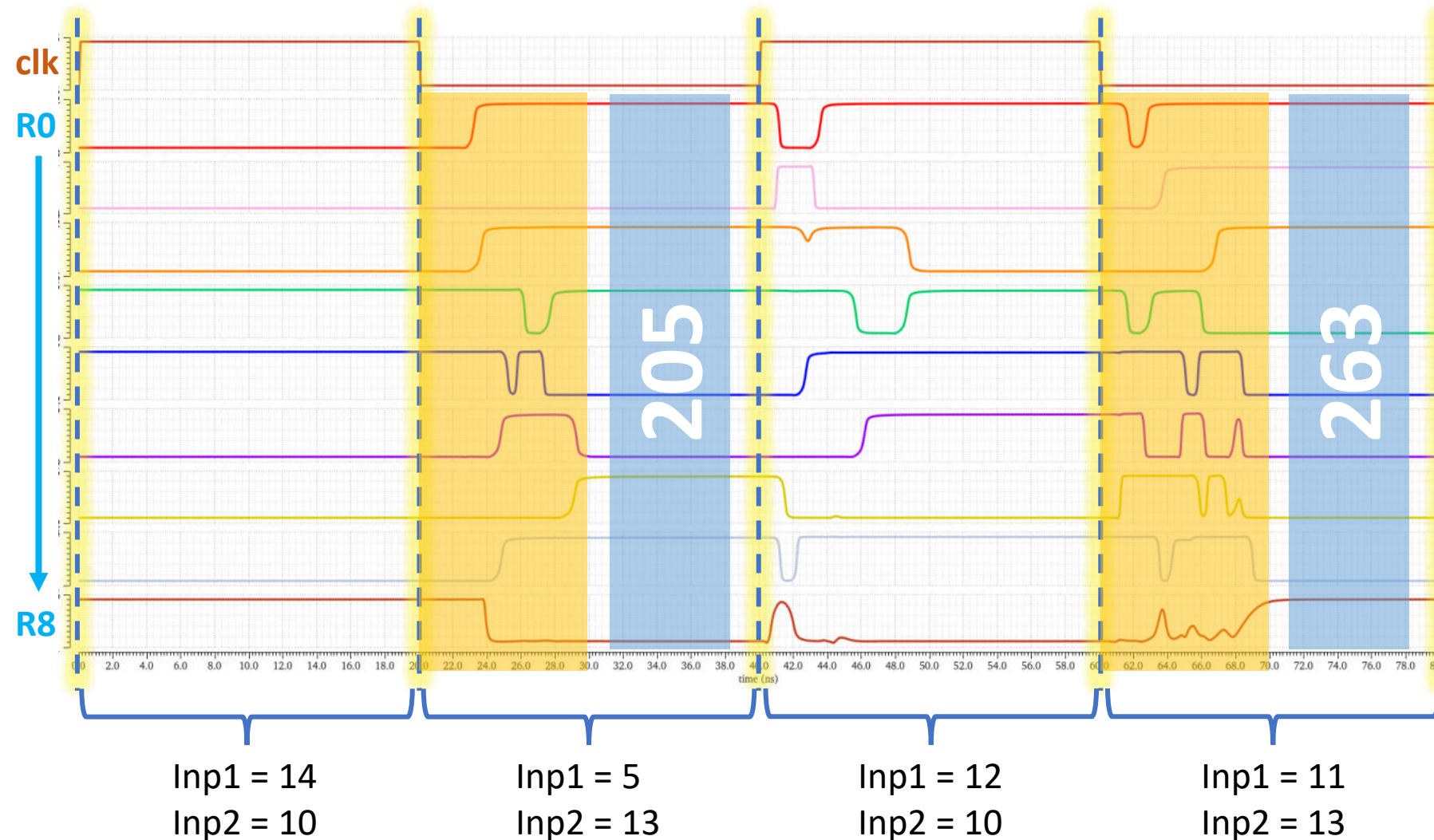


Extracted

Transistor Count			
Module	#Unit	FET/unit	Total FET
Multiplier	1	736	736
D-Latch	16	6	96
CLA4	2	134	268
INV2	1	2	2
Aggregate Count			1102

Total Area = $297.75\ \mu m \times 204\ \mu m$
= $0.0607\ mm^2$

continued...



□ Test Case:

$$\begin{bmatrix} 14 & 5 \\ 12 & 11 \end{bmatrix} \cdot \begin{bmatrix} 10 \\ 13 \end{bmatrix} = \begin{bmatrix} 205 \\ 263 \end{bmatrix}$$

■ 205 = b0_1100_1101

■ 263 = b1_0000_0111

Note:

- clk frequency is 25 MHz here.
 - can be increased up to 45 MHz
- t_{pd} is 9 ns.

Conclusion

Problems we faced

- Only up to M3 was available.
- Too much emphasis upon equal R_{rise} & R_{fall}
- D-FF or D-Latch?
- Placement of last CLA after D-Latch
- OAI54321: Height vs. Width

Problems in our design

- 4x4 Multiplier
 - Unnecessary \overline{P} , \overline{G} from last CLA4
 - Unnecessary XNOR2 gates at peripheral
- Final design
 - Not running at 80 MHz as predicted

Questions?
Concerns?
Comments?