CMOS Matrix-Vector Multiplier

ECE 533 – Project Design Review

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- Tanjina Sabrin
- Md Farhan

Brief Outline

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \cdot \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} ax + by \\ cx + dy \end{bmatrix}$$

Input:

- a, b, c, d, x, y → 4-bit unsigned each

Product:

- ax, by, cx, dy → 8-bit unsigned each

Output:

- $(ax + by), (cx + dy)$ → 9-bit unsigned

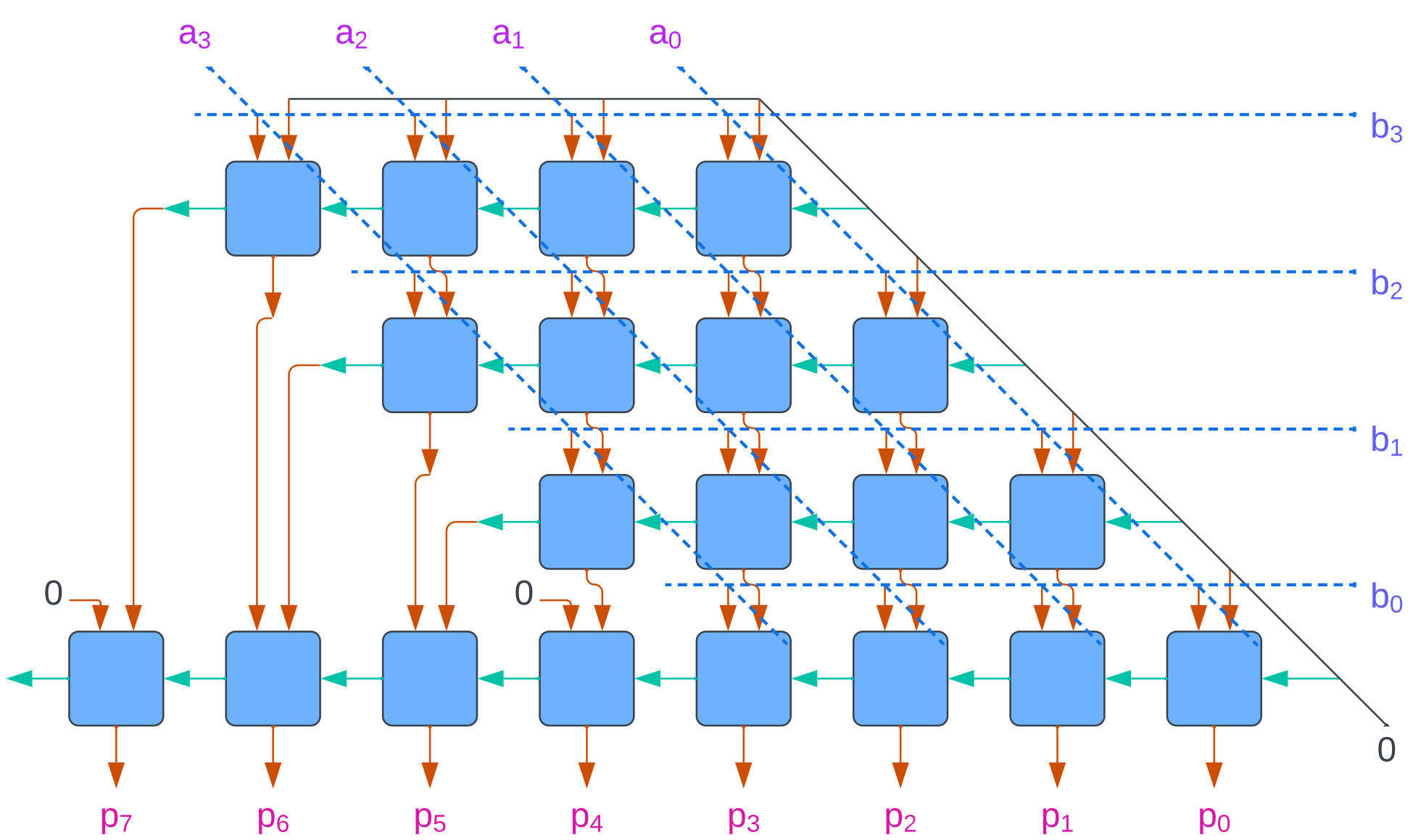
What we need:

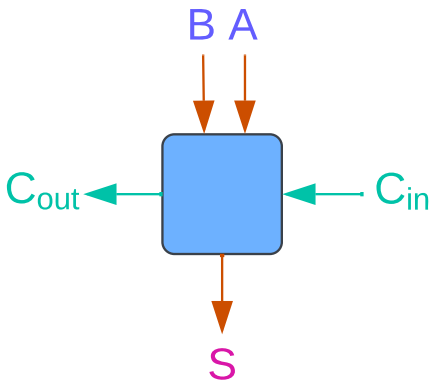
- 4×4 Multiplier
- 8-bit Adder
- Banks of D-Latch

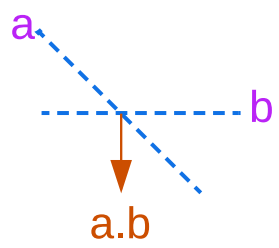
Adder Type:

- Carry-lookahead Adder (CLA)

4x4 Unsigned Multiplier







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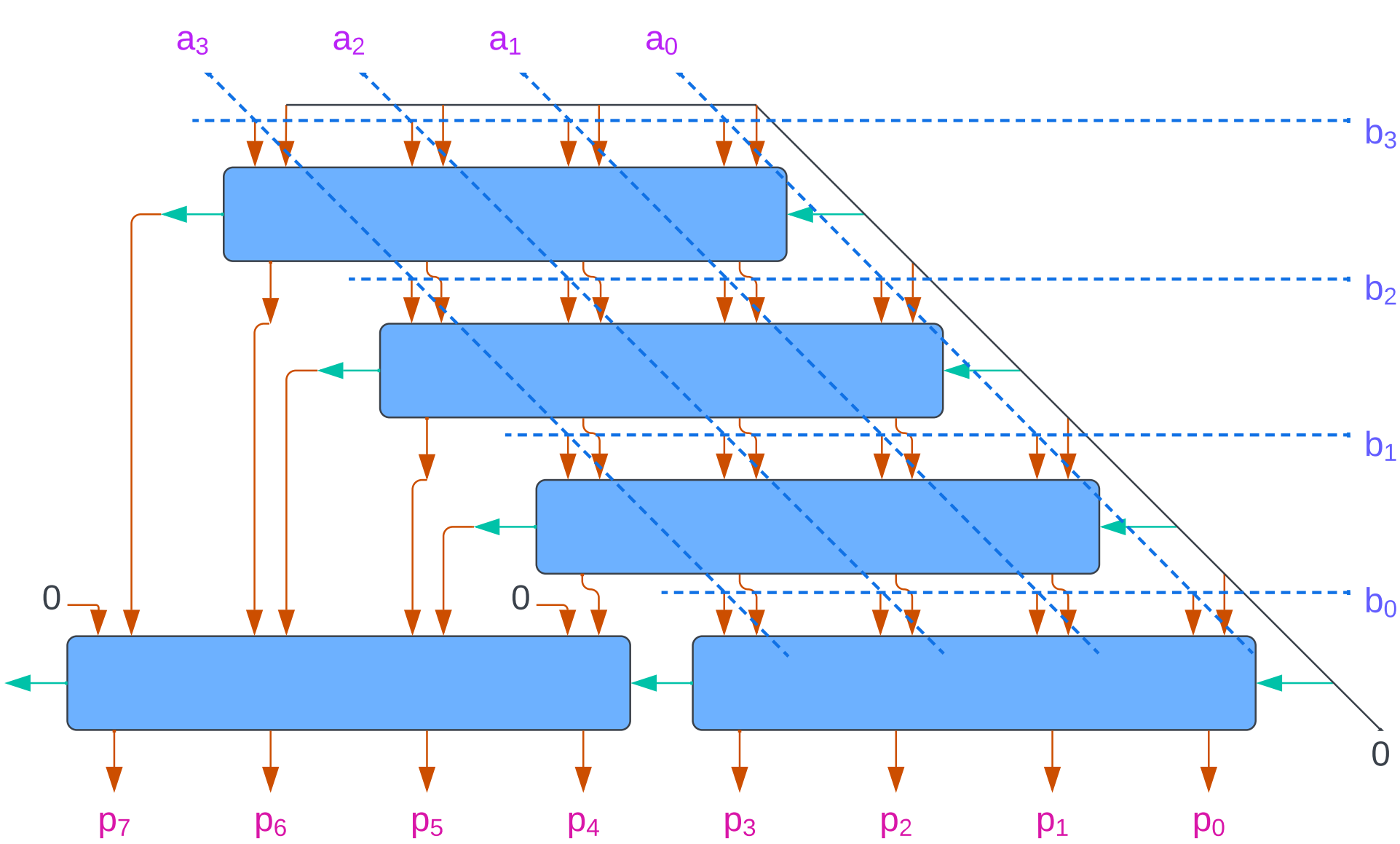
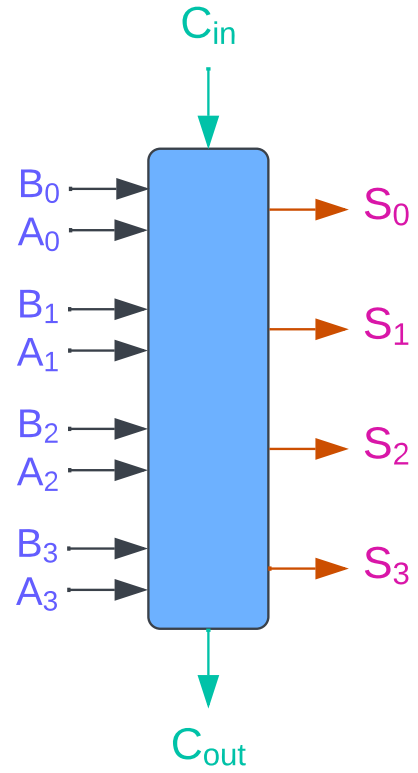
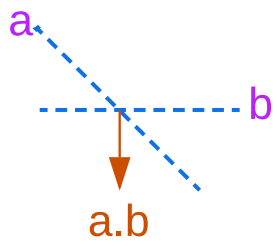

a3
a2
a1
a0
b3
b2
b1
b0
0
0
0
p7
p6
p5
p4
p3
p2
p1
p0


Cin
B0
A0
B1
A1
B2
A2
B3
A3
S0
S1
S2
S3
Cout


a
b
a.b

Propagate & Generate (PG) Logic

A	B	C_{in}	C_{out}	S	P	G
0	0	0	0	0	0	0
		1	0	1		
0	1	0	0	1	1	0
		1	1	0		
1	0	0	0	1	1	0
		1	1	0		
1	1	0	1	0	0	1
		1	1	1		

Propagate:

- C_{out} is true if C_{in} is true.

$$P = A \oplus B$$

Generate:

- C_{out} is true.

$$G = A \cdot B$$

$$S = (A \oplus B) \oplus C_{in} = P \oplus C_{in}$$

$$C_{out} = G + P \cdot C_{in}$$

continued…

- Generalized formula:

$$C_{i+1} = G_i + P_i \cdot C_i$$

- For 4-bit CLA unit:

$$C_1 = G_0 + P_0 \cdot C_0$$

$$C_2 = G_1 + P_1 \cdot C_1$$
$$= G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1$$

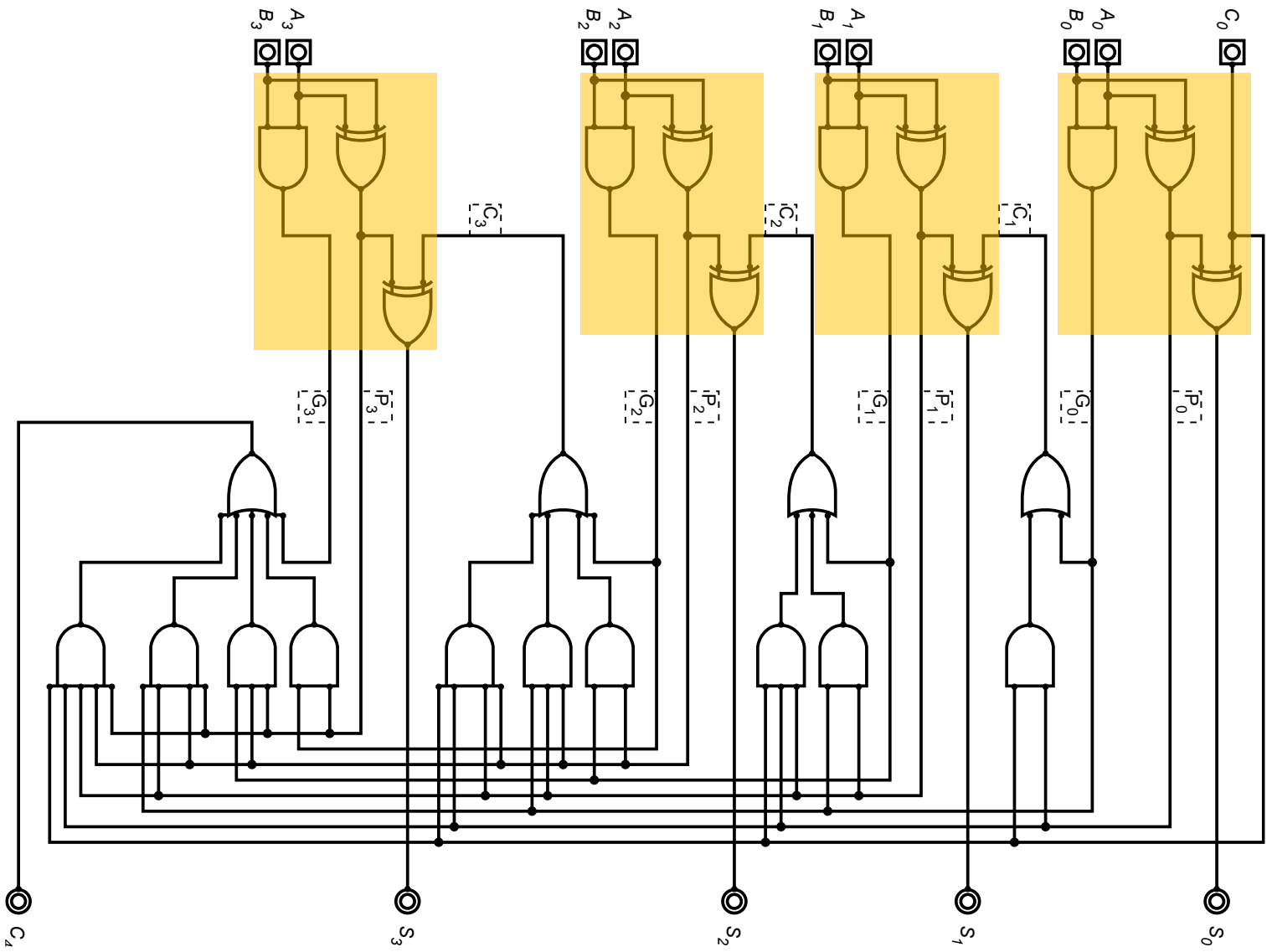
$$C_3 = G_2 + P_2 \cdot C_2$$
$$= G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2$$

$$C_4 = G_3 + P_3 \cdot C_3$$
$$= G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3$$

Remember:

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \cdot B_i$$

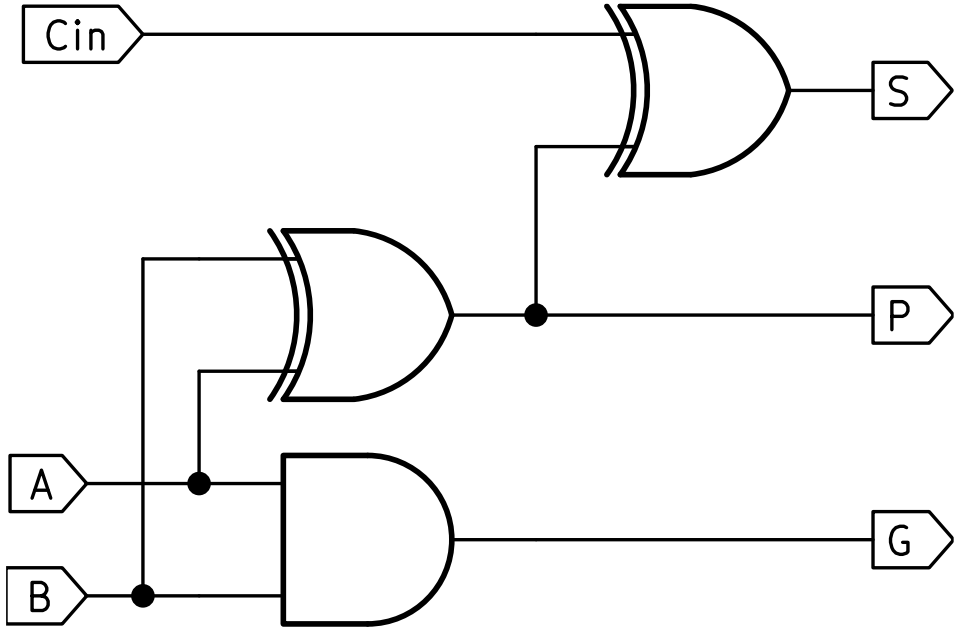
4-bit CLA unit (*unoptimized*)

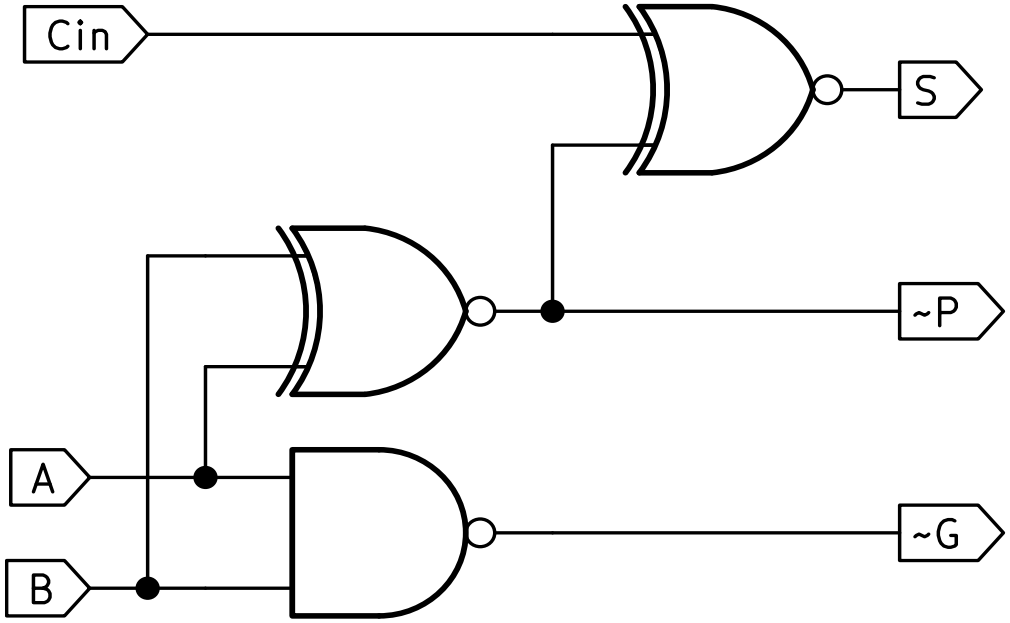


Transistor Count			
Gate	**#Unit**	**FET/unit**	**Total FET**
XOR2	8	6	48
AND2	8	6	48
AND3	3	8	24
AND4	2	10	20
AND5	1	12	12
OR2	1	6	6
OR3	1	8	8
OR4	1	10	10
OR5	1	12	12
Aggregate Count			**188**

Note: *Inputs are unavailable in complemented form.*

Road to Optimization



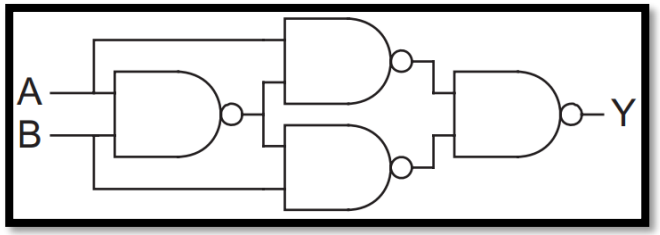


Transistor Count			
Gate	**#Unit**	**FET/unit**	**Total FET**
XOR2	2	6	12
AND2	1	6	6
Aggregate Count			**18**

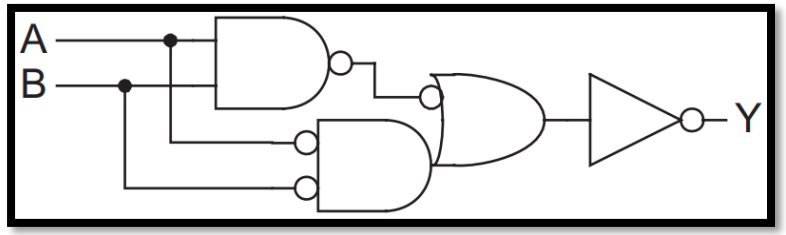
Transistor Count			
Gate	**#Unit**	**FET/unit**	**Total FET**
XNOR2	2	6	12
NAND2	1	4	4
Aggregate Count			**16**

continued…

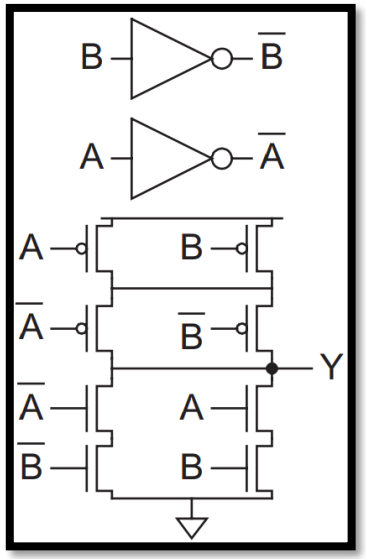
XOR2 Designs



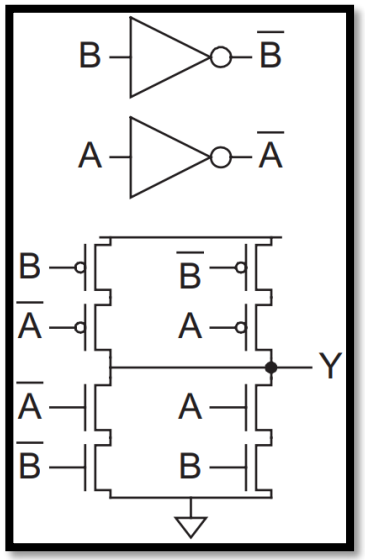
16 T



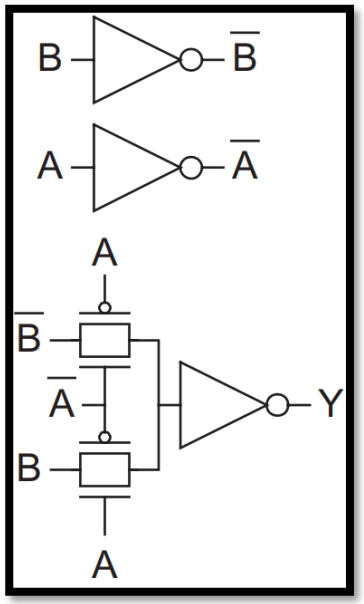
12 T



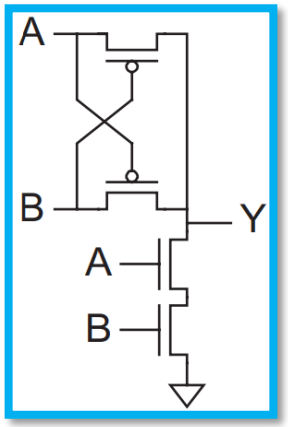
12 T



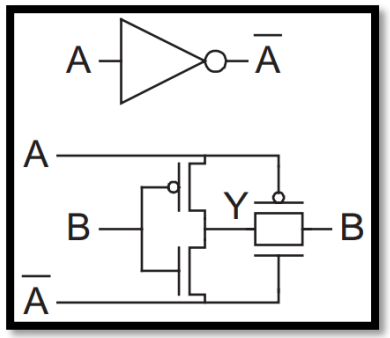
12 T



10 T



4 T



6 T

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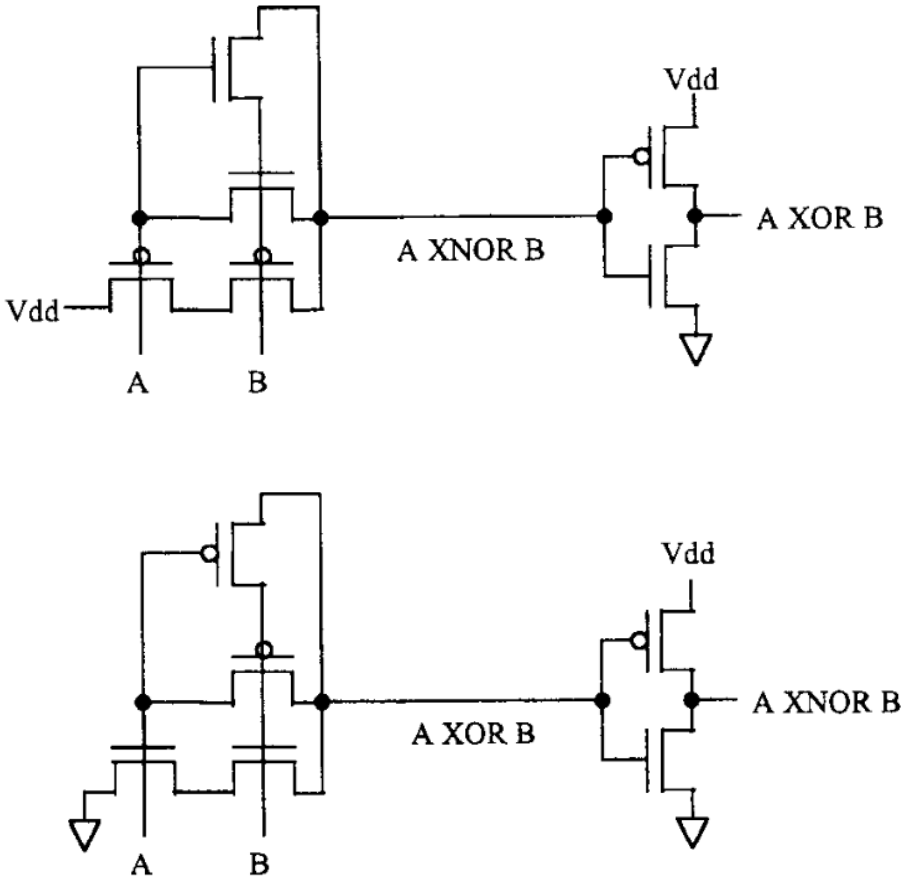
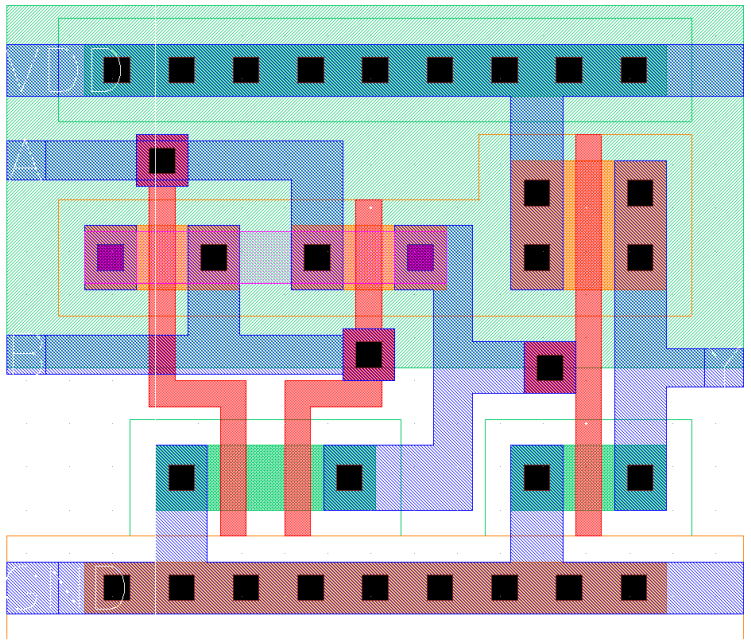
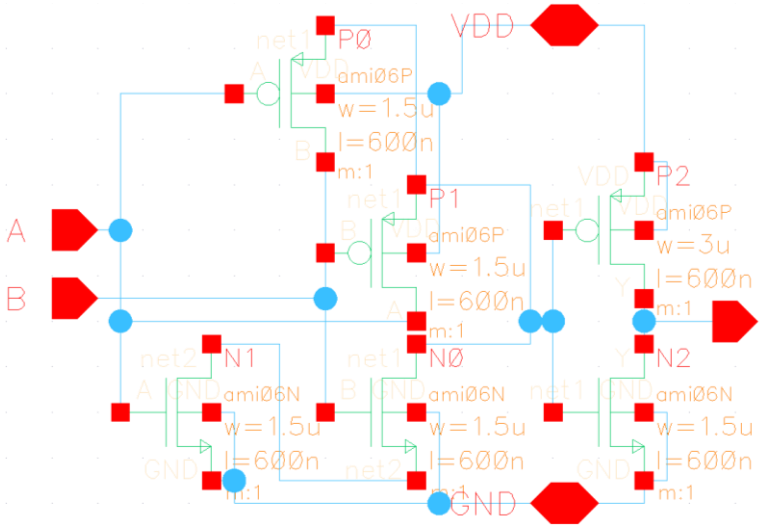


Ref: J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," in *IEEE Journal of Solid-State Circuits*, vol. 29, no. 7, pp. 780-786, July 1994, doi: 10.1109/4.303715.

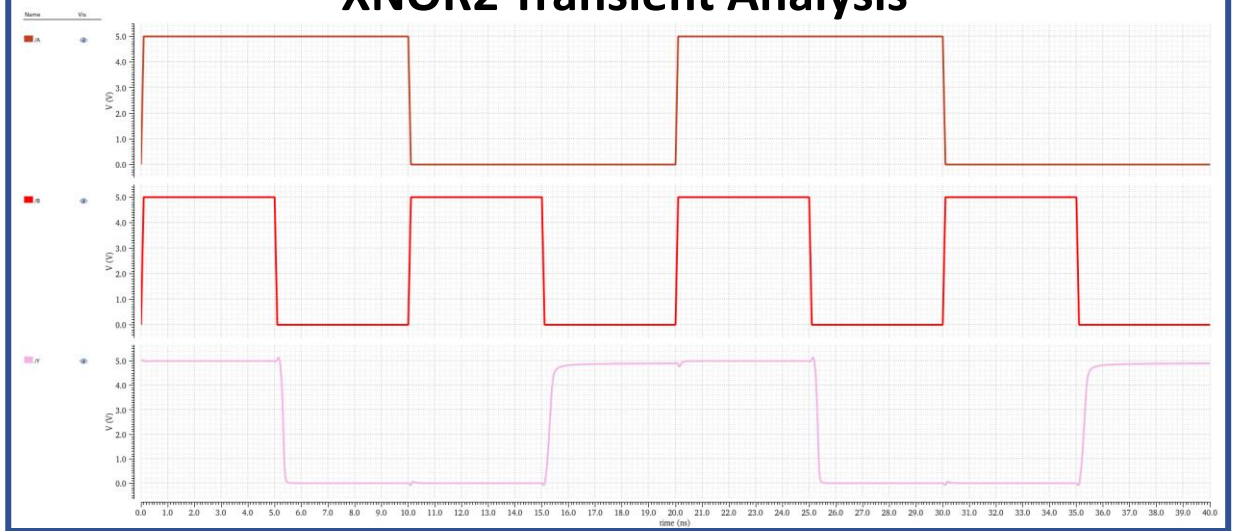
XNOR2 Layout



XNOR2 Schematic



XNOR2 Transient Analysis



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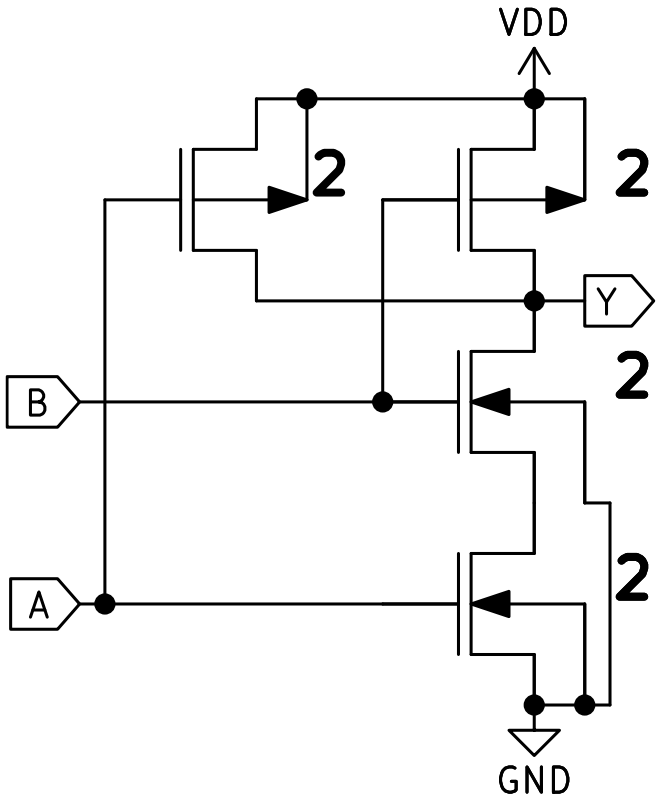
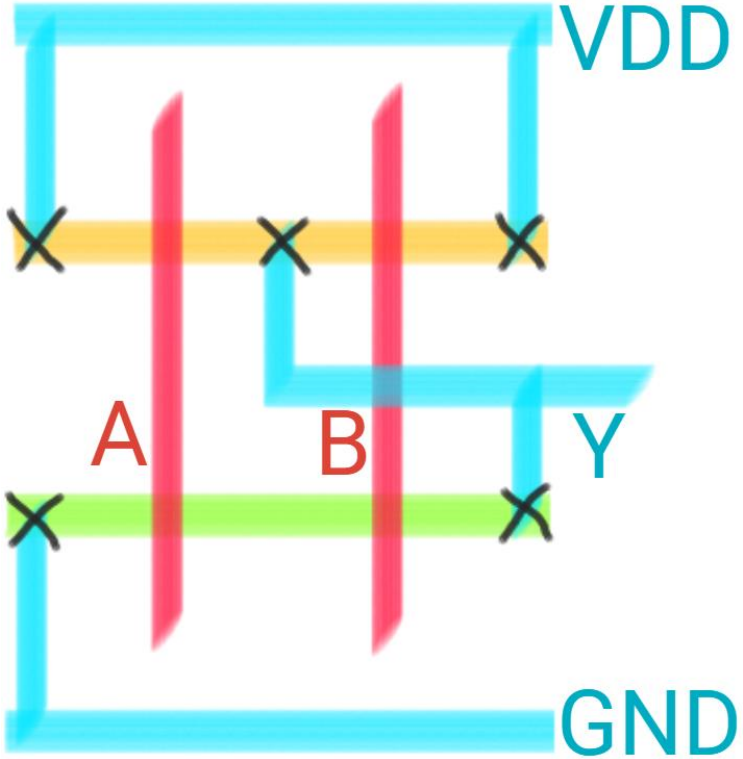
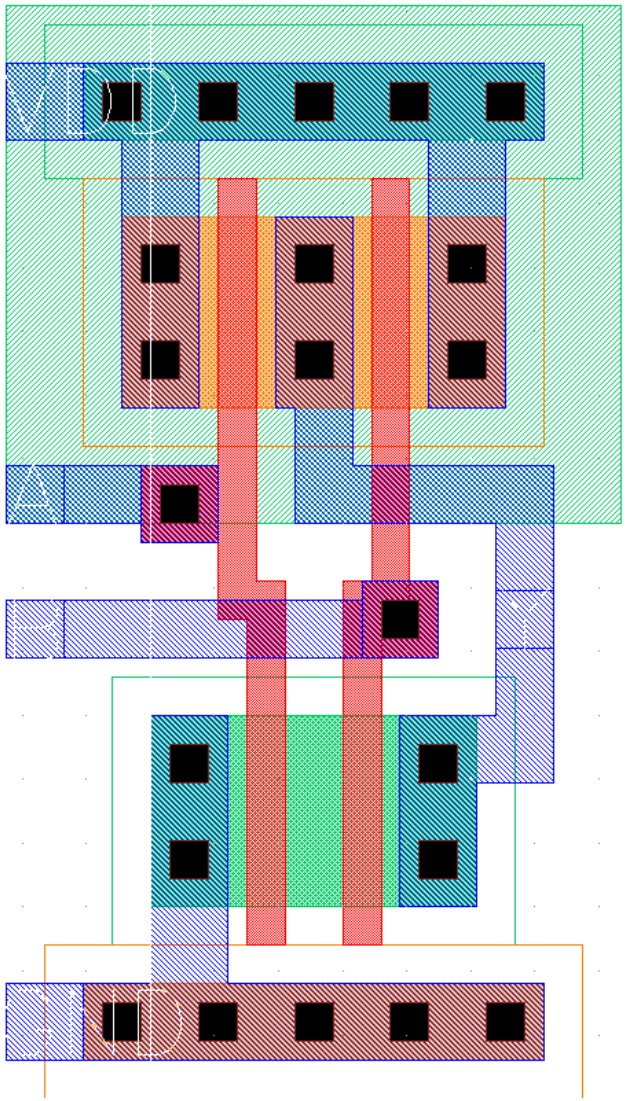
NAND2 Schematic



NAND2 Stick Diagram



NAND2 Layout



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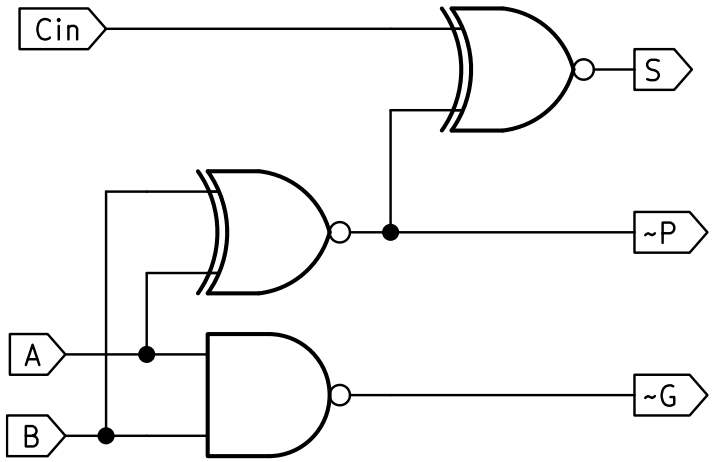
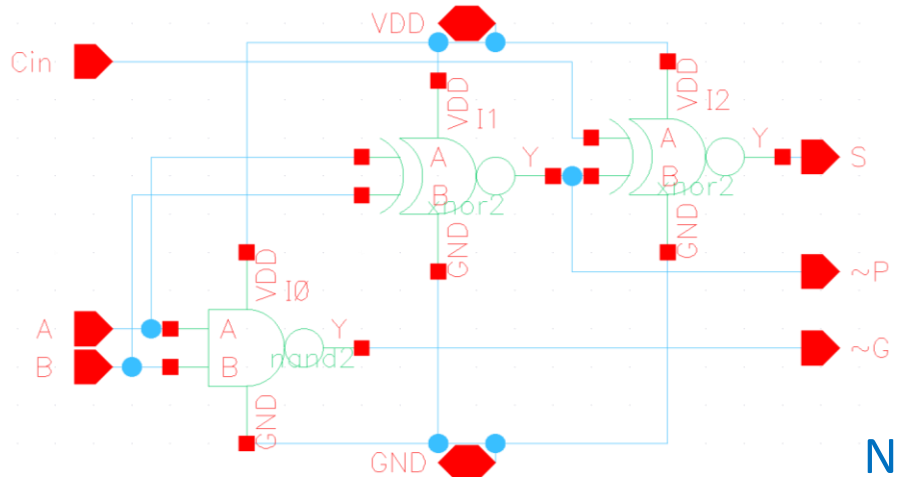
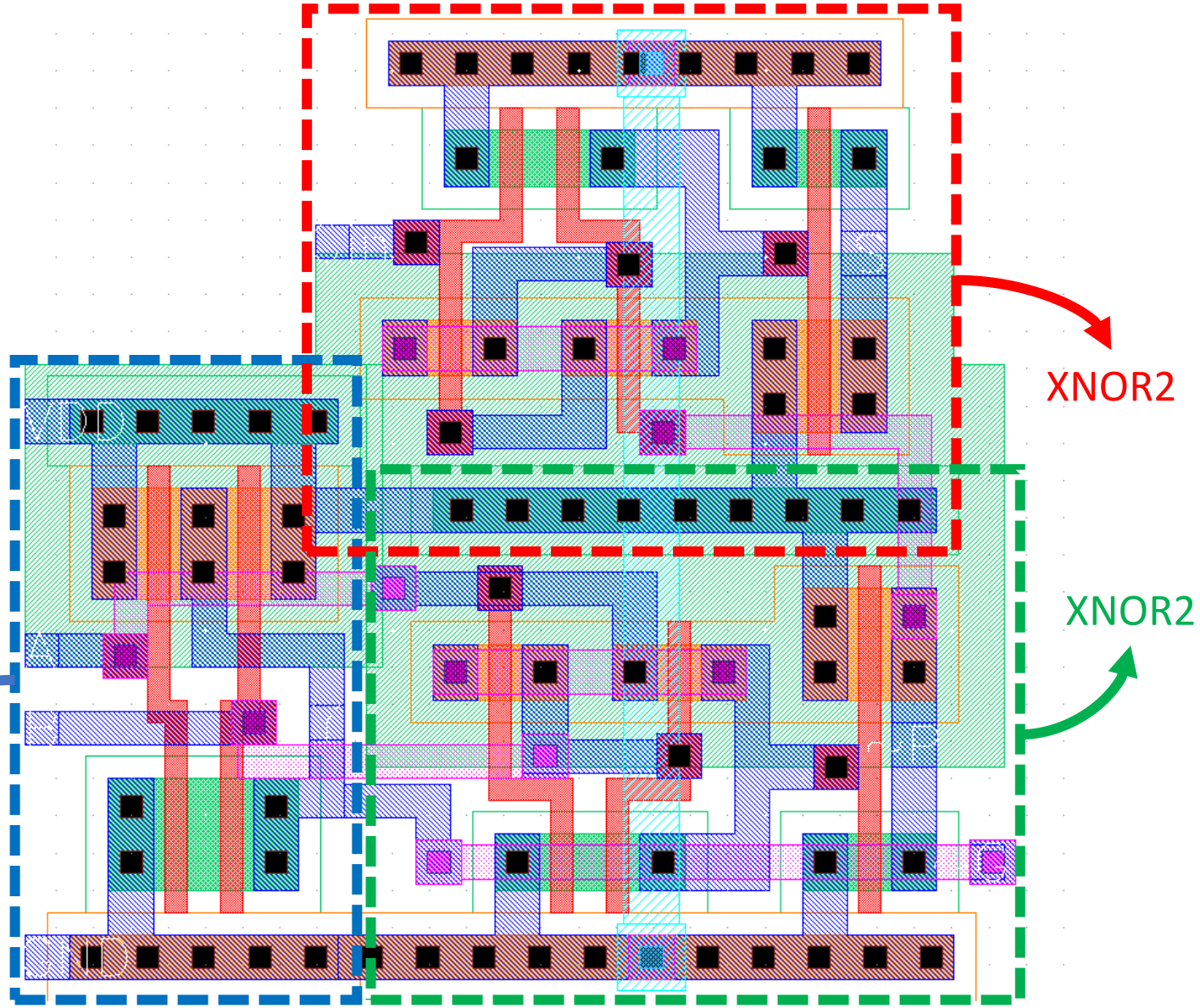
SPG unit Schematic





SPG unit Layout



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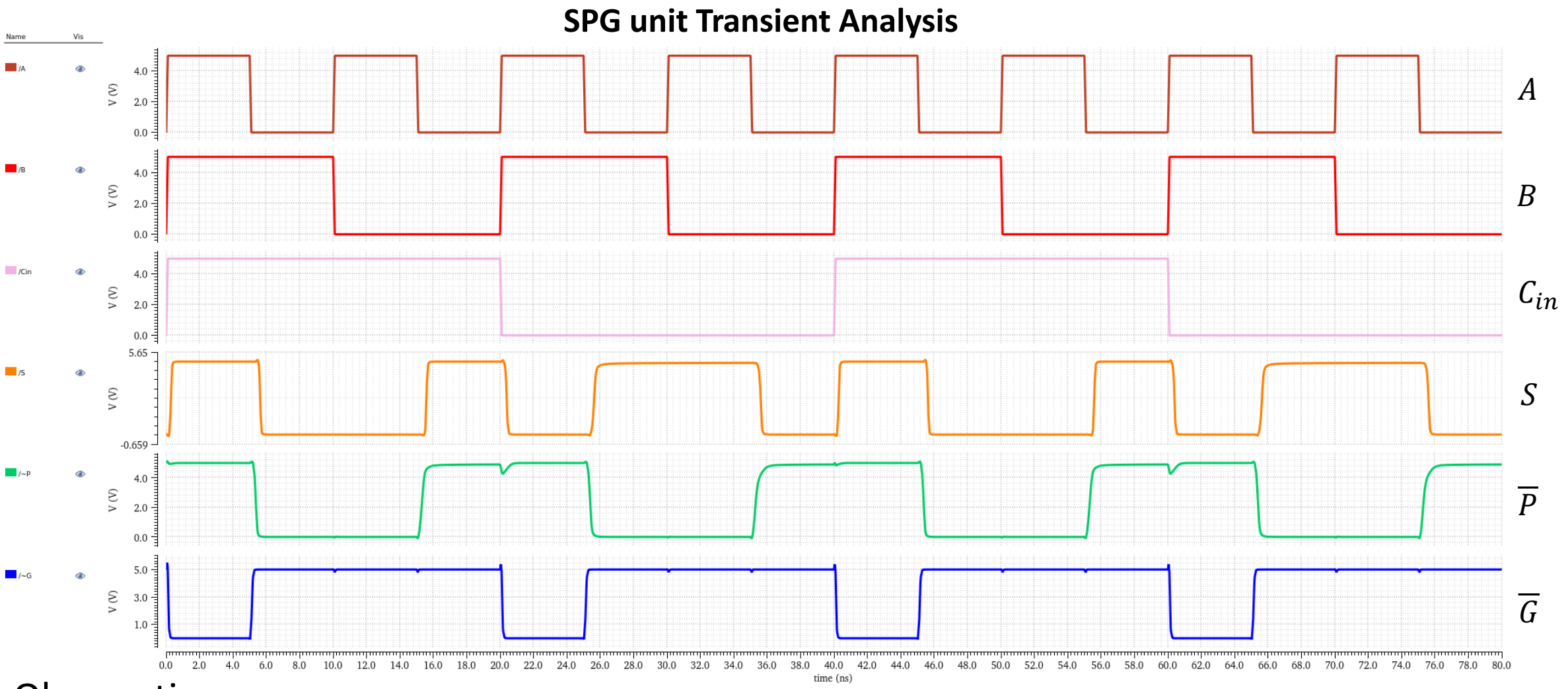
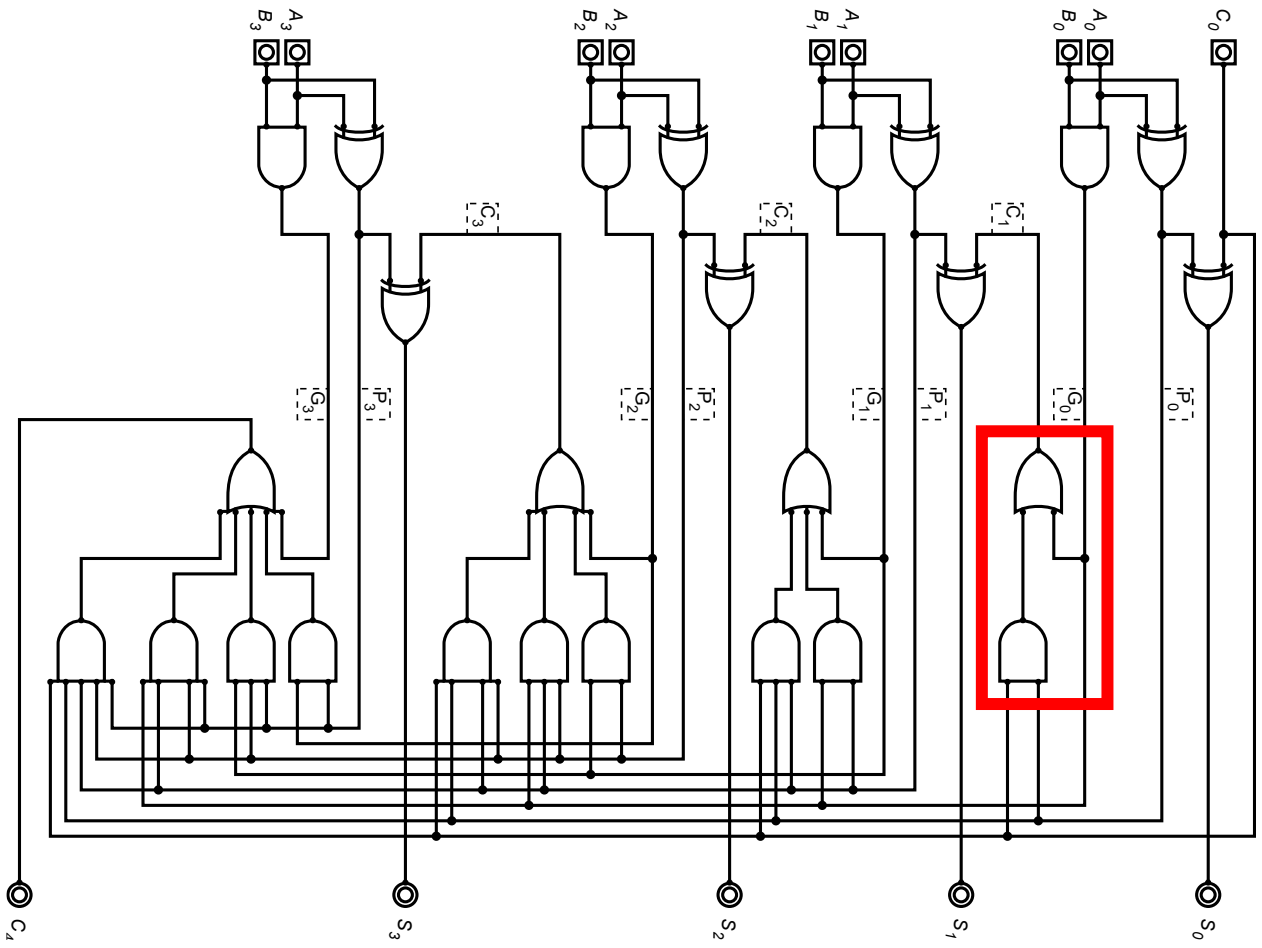


Observation:

- S is slowest, $\overline{G}$ is fastest.
- $\overline{P}$, $\overline{G}$ can be directly used for next PG blocks instead of P , G. (But how?)

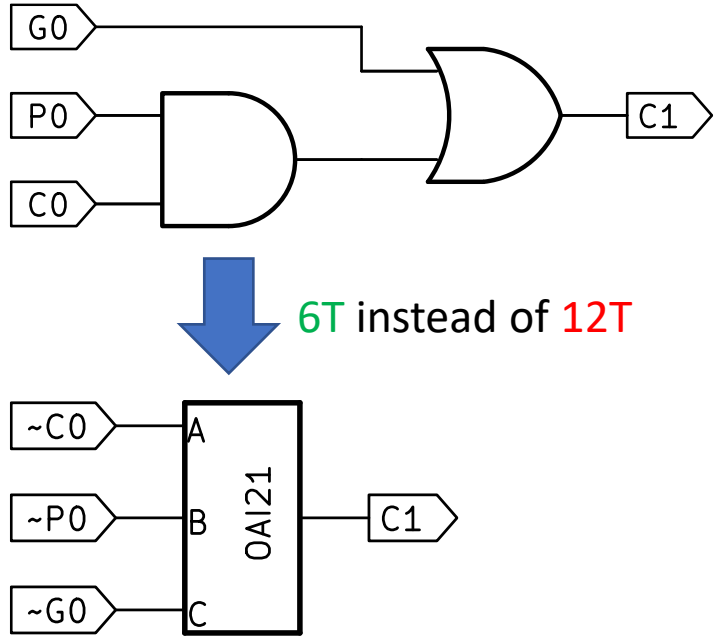
PG Logic: 1st Stage



$$C_1 = G_0 + P_0 \cdot C_0$$

$$= \overline{\overline{G_0 + P_0 \cdot C_0}}$$

$$= \overline{\overline{G_0} \cdot \left(\overline{P_0} + \overline{C_0}\right)} \rightarrow \text{OAI21}$$



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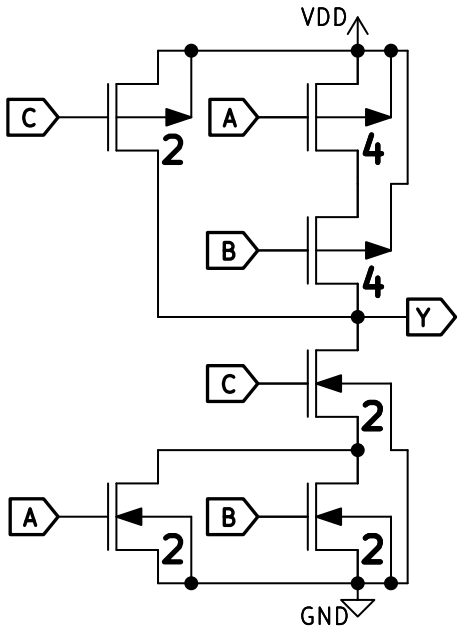
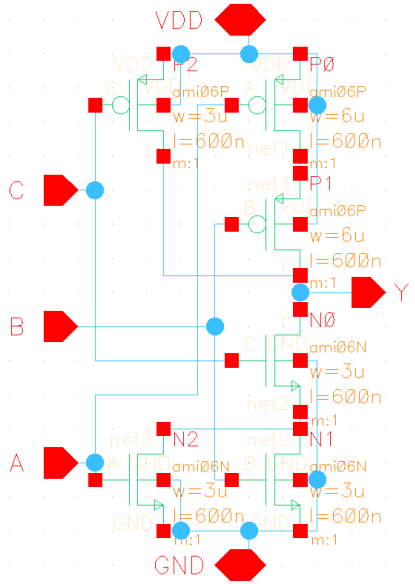
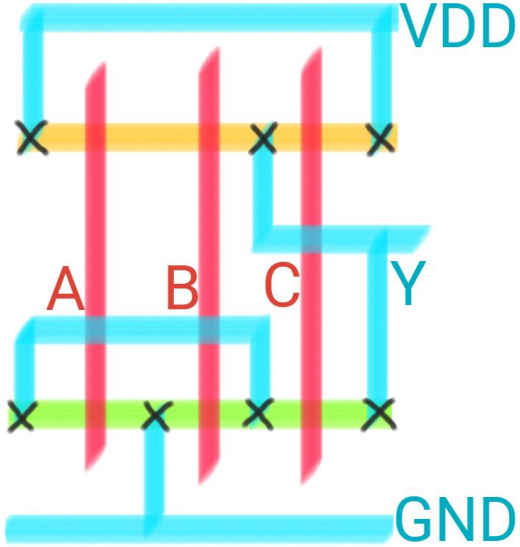
OAI21 Schematic

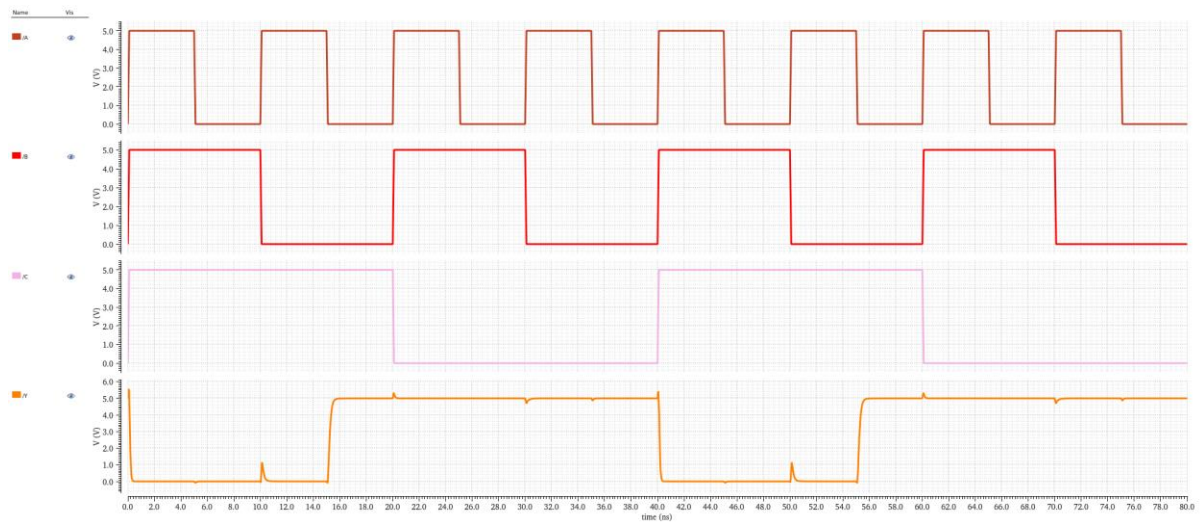




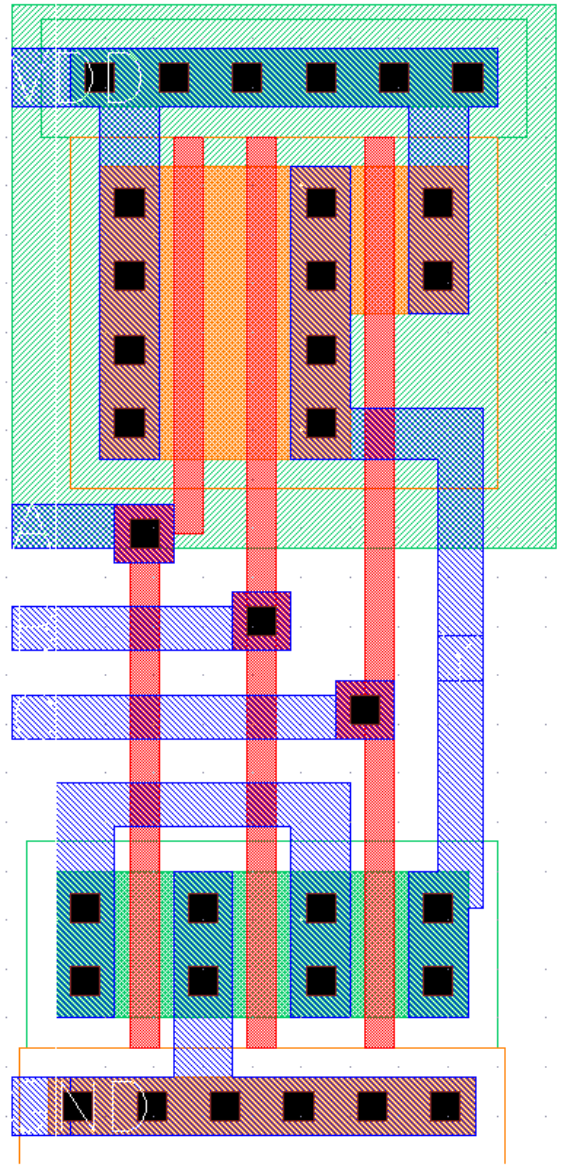
OAI21 Stick Diagram



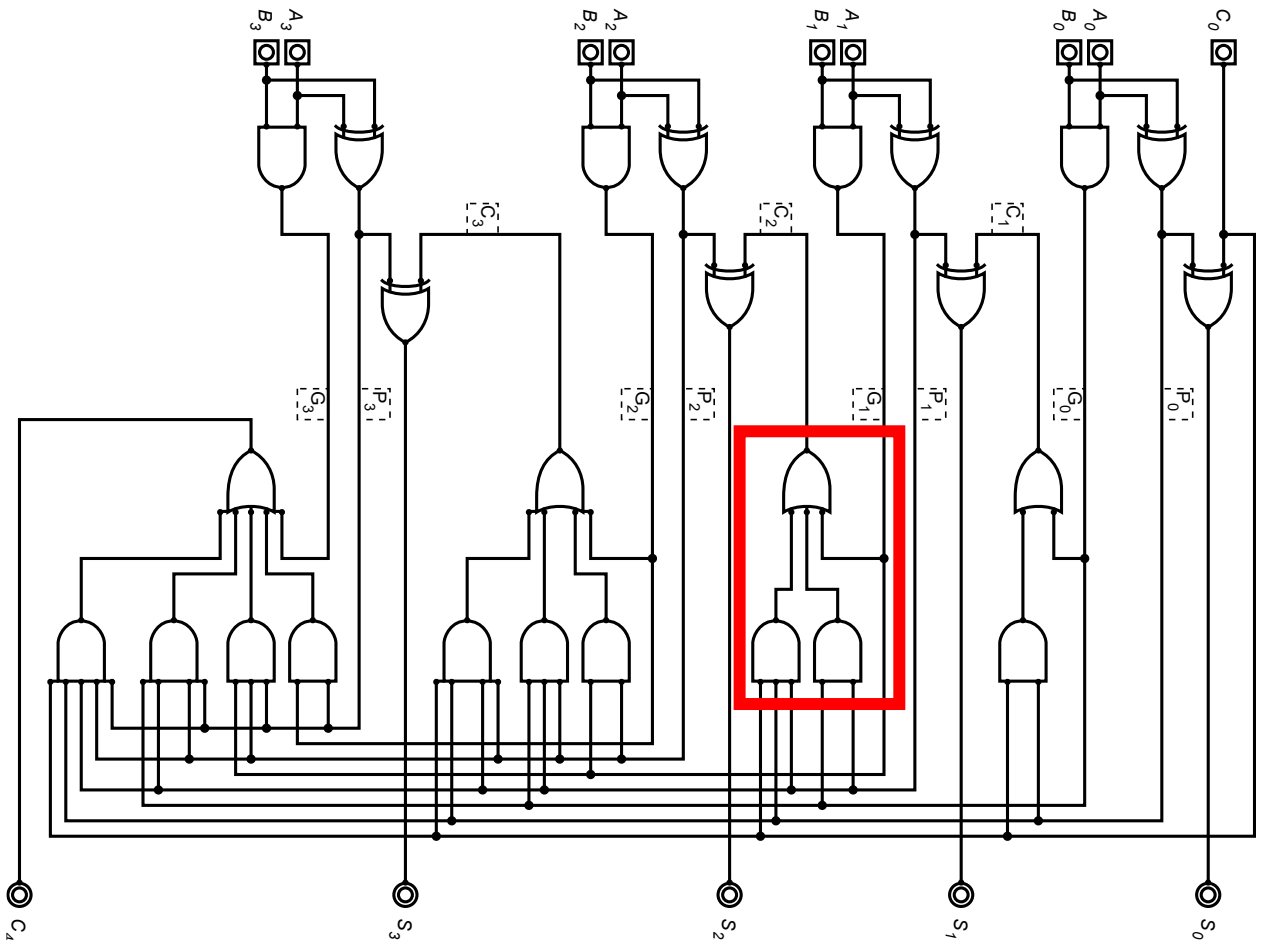
OAI21 Transient Analysis



OAI21 Layout



PG Logic: 2nd Stage

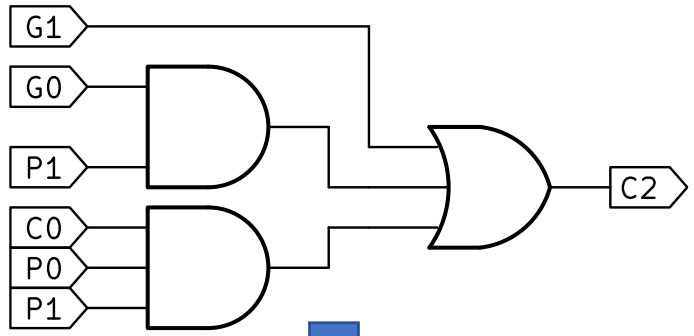


$$C_2 = G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1$$

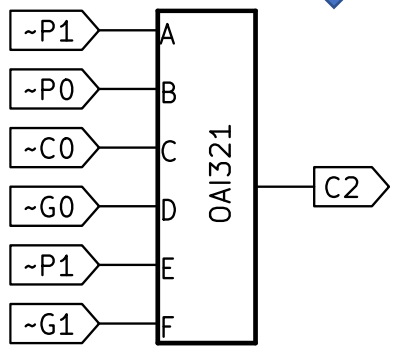
$$= \overline{\overline{G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1}}$$

$$= \overline{\overline{G_1} \cdot \left(\overline{G_0} + \overline{P_1}\right) \cdot \left(\overline{C_0} + \overline{P_0} + \overline{P_1}\right)}$$

↪ OAI321



12T instead of 22T



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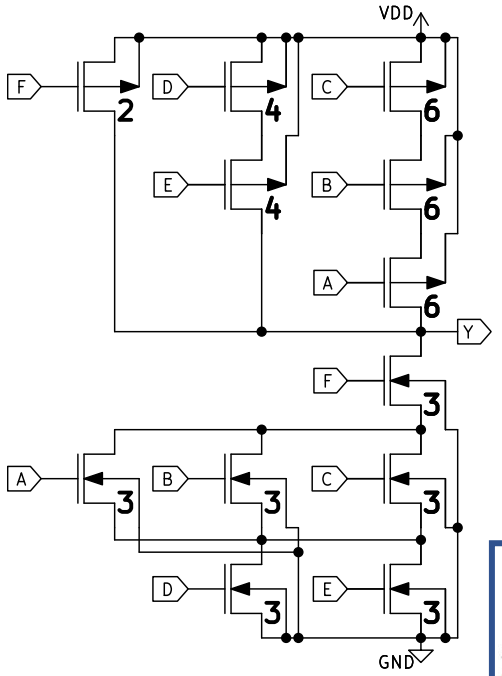
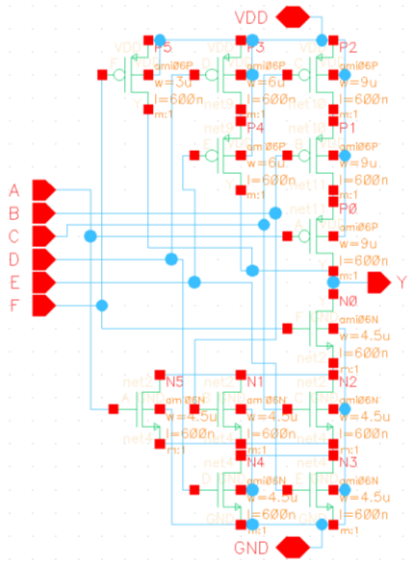
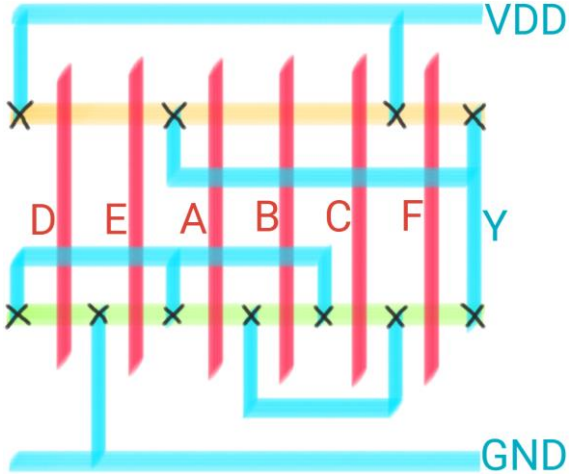
OAI321 Schematic

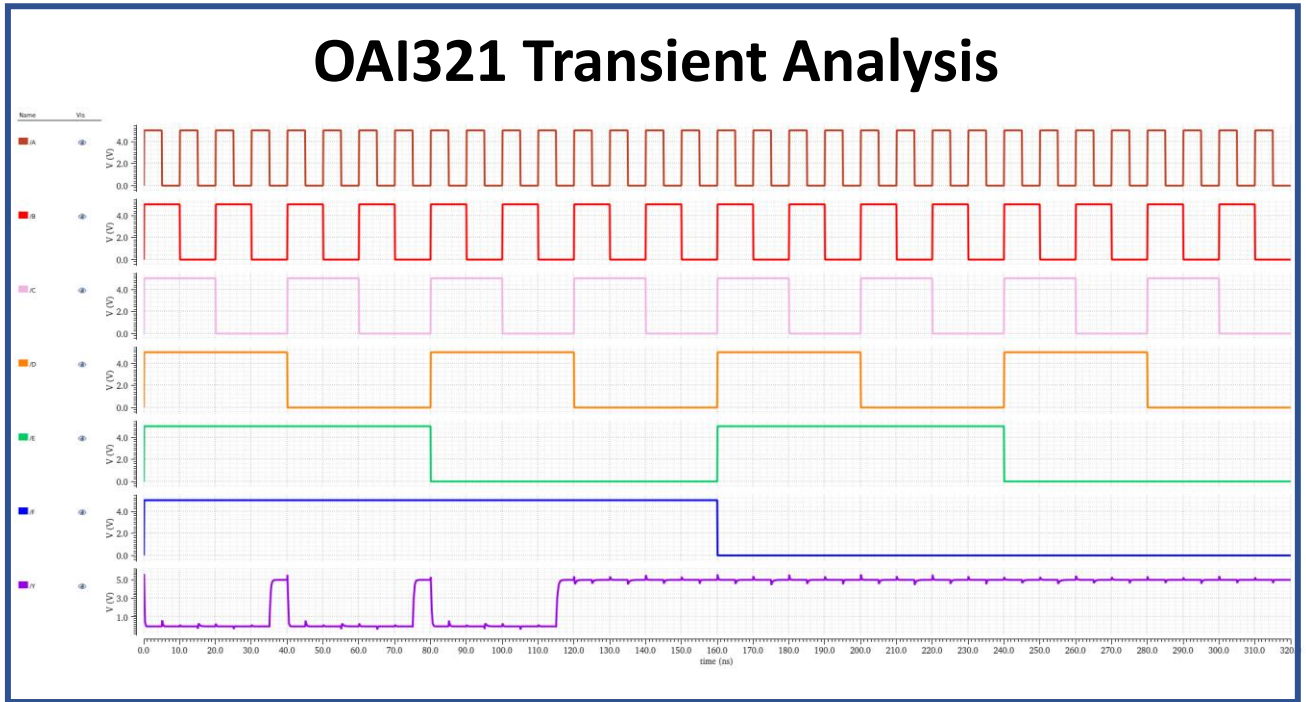




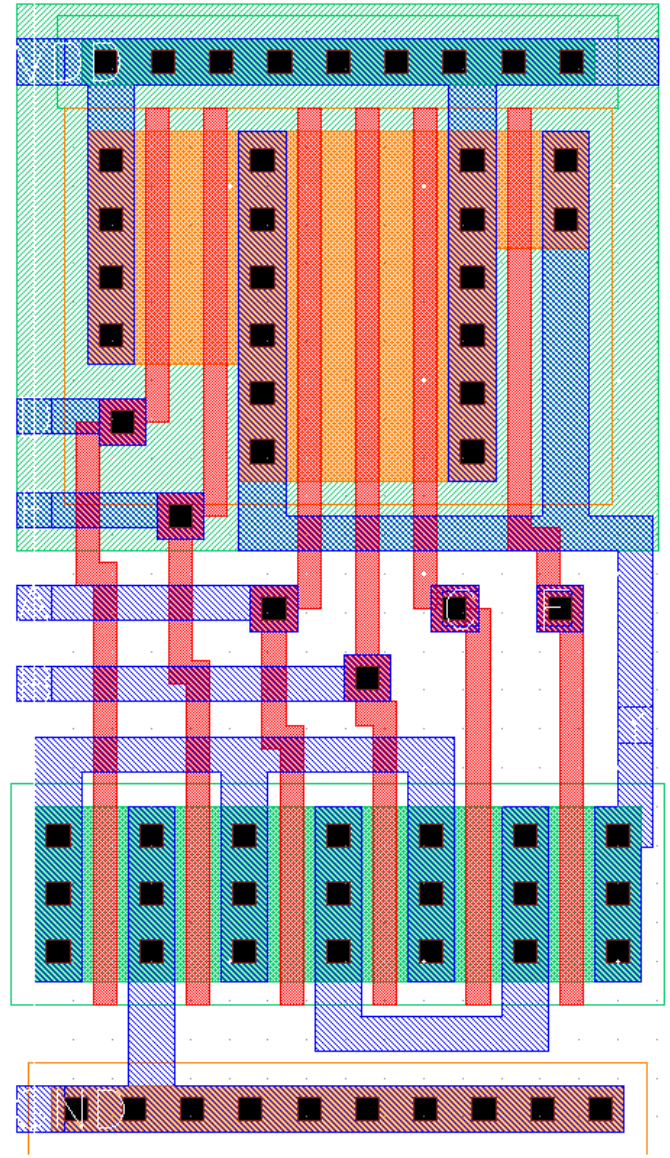
OAI321 Stick Diagram



OAI321 Transient Analysis



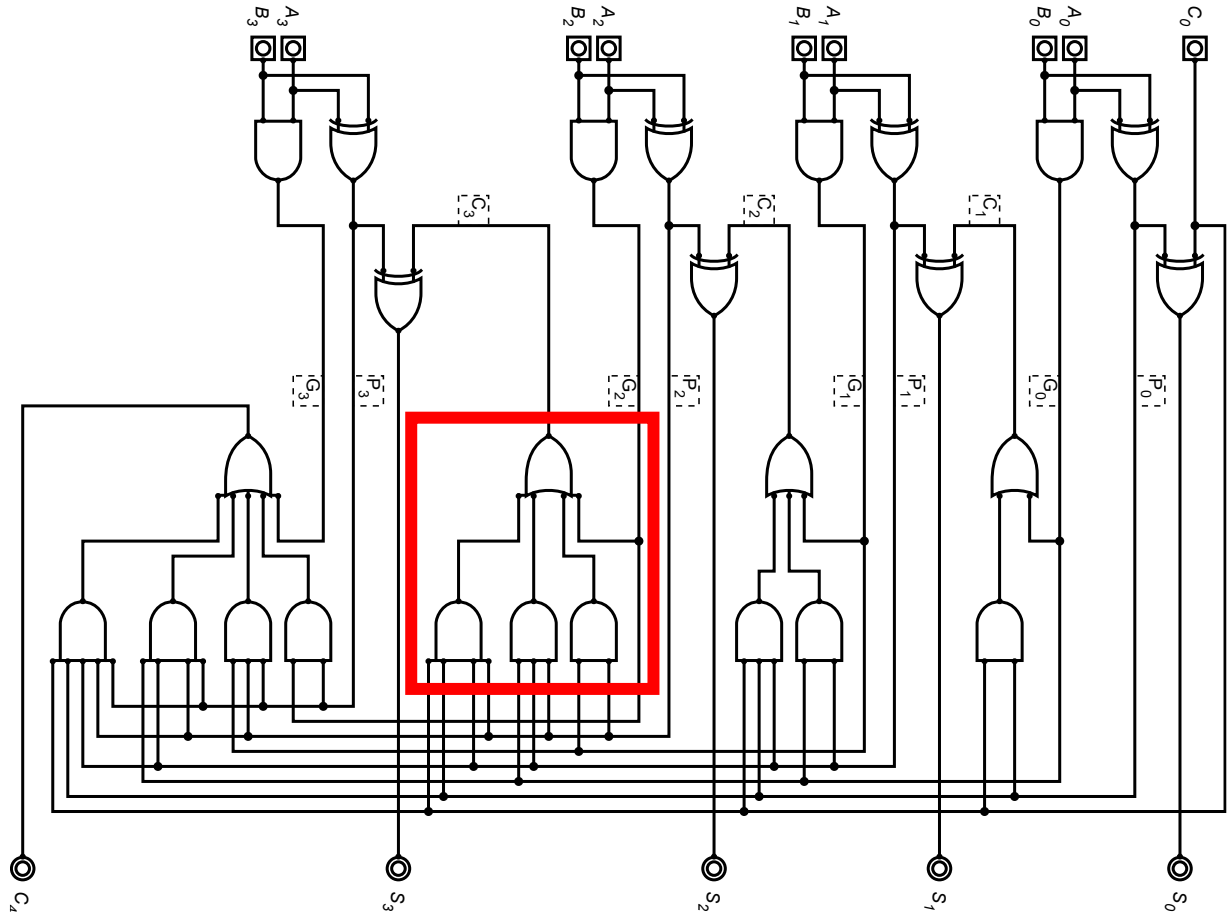
OAI321 Layout

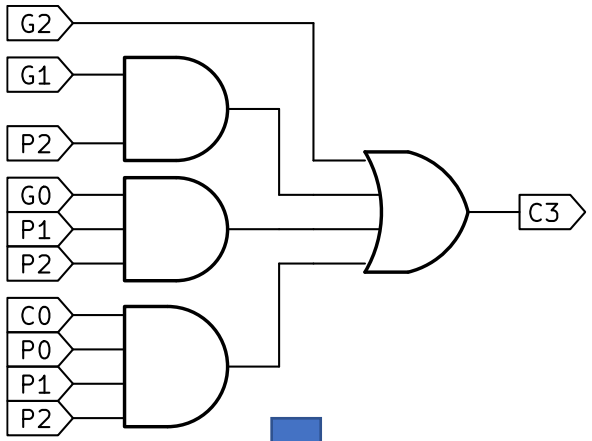


PG Logic: 3rd Stage

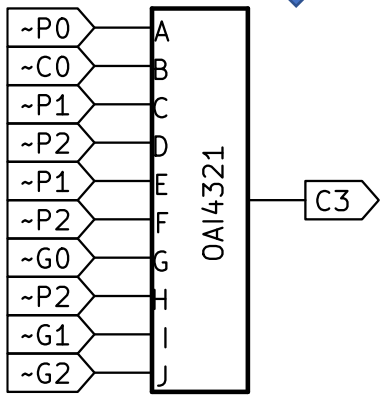
$$C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2$$
$$= \overline{G_2} \cdot \left(\overline{G_1} + \overline{P_2}\right) \cdot \left(\overline{G_0} + \overline{P_1} + \overline{P_2}\right) \cdot \left(\overline{C_0} + \overline{P_0} + \overline{P_1} + \overline{P_2}\right)$$

↪ OAI4321





20T instead of 34T



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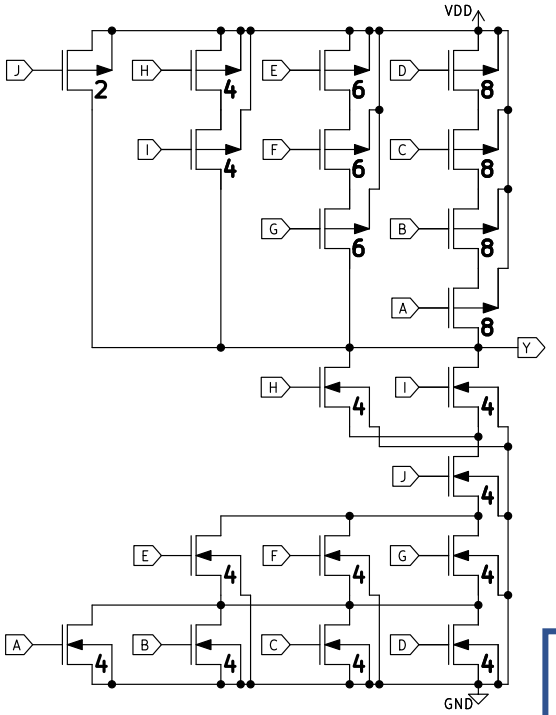
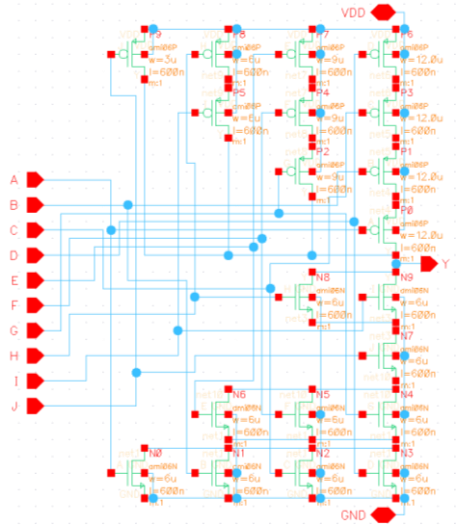
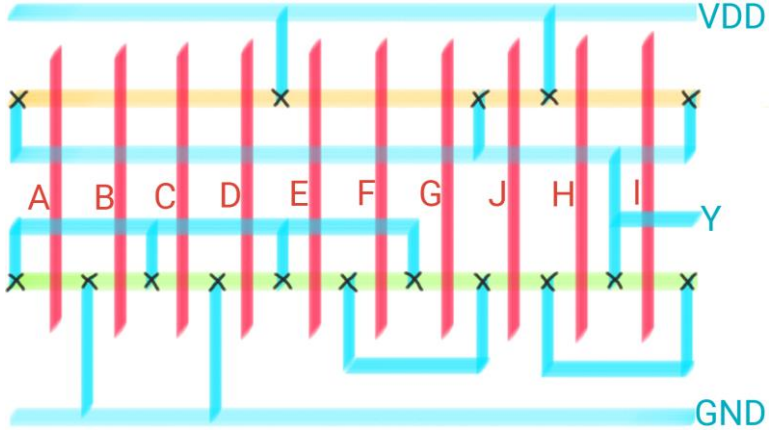
OAI4321 Schematic



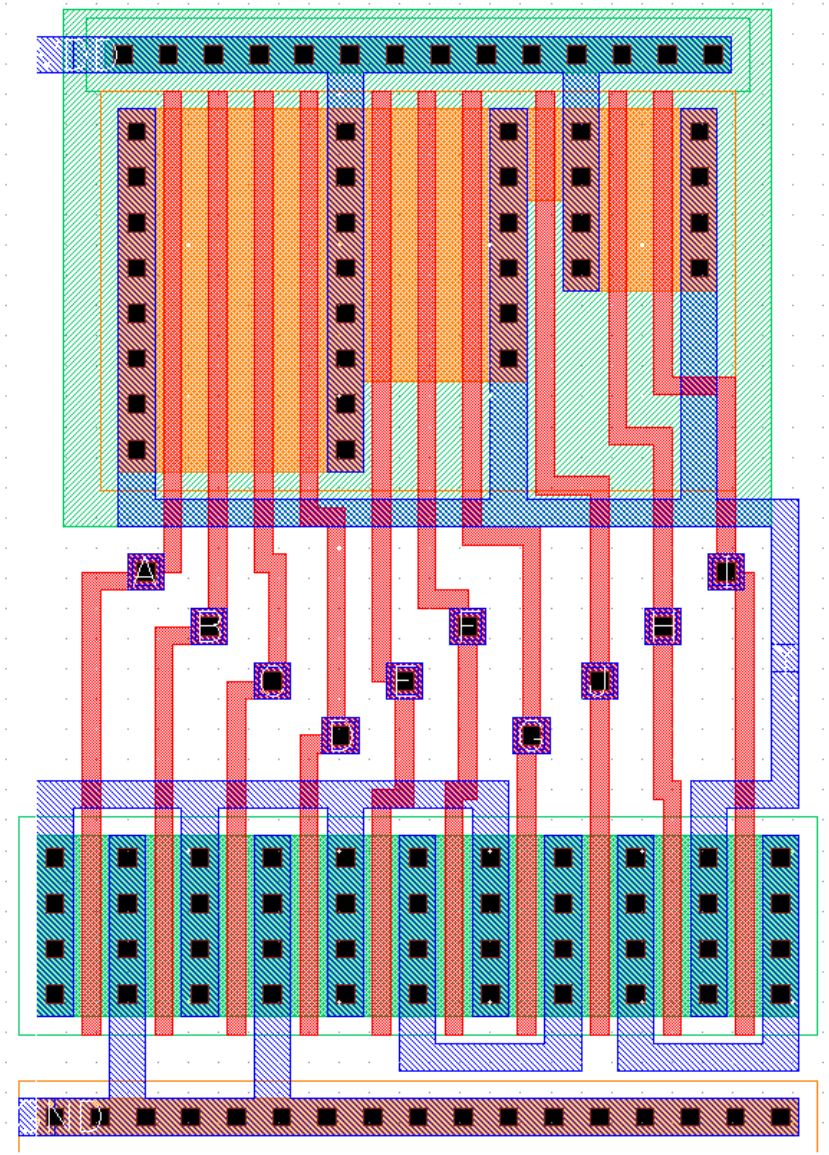


OAI4321 Stick Diagram



OAI4321 Transient Analysis (*cropped*)

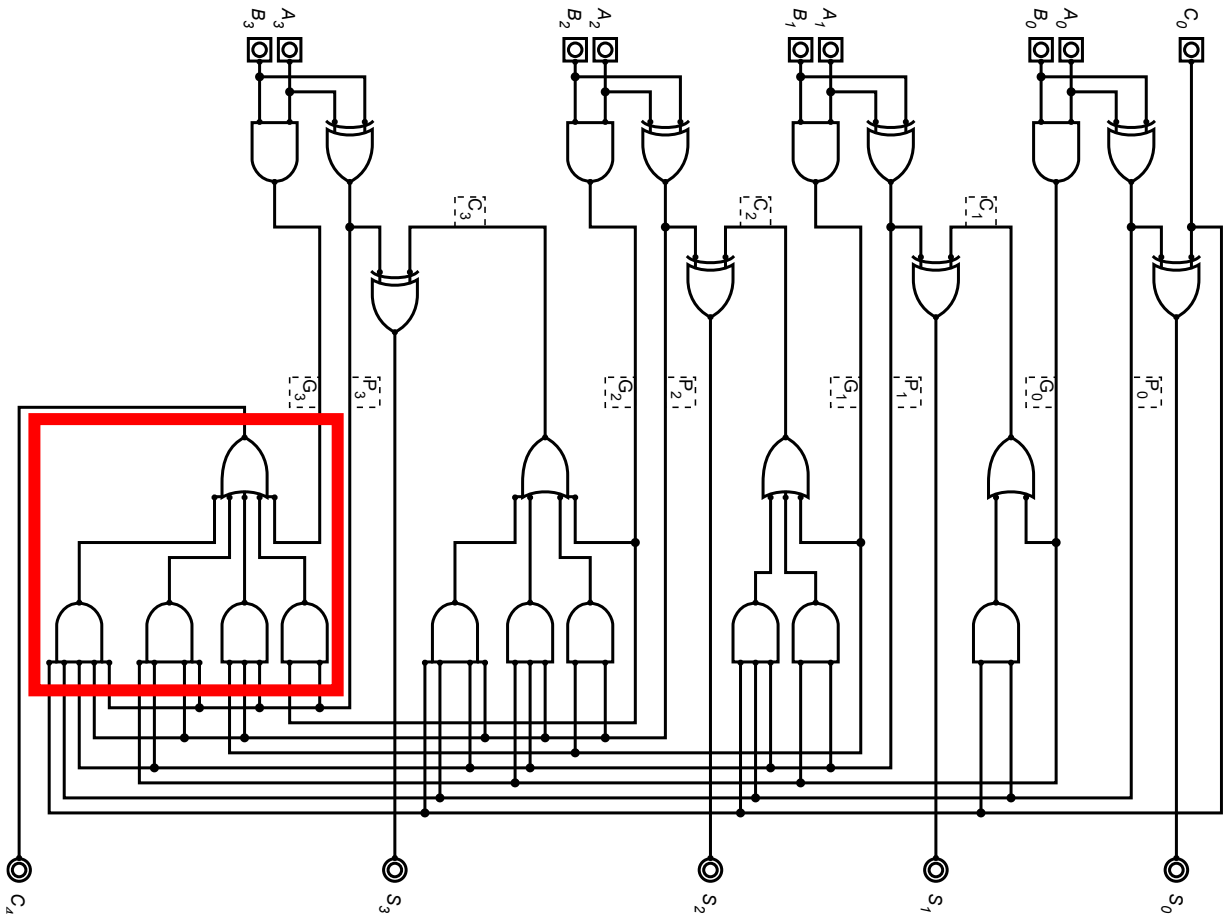
OAI4321 Layout

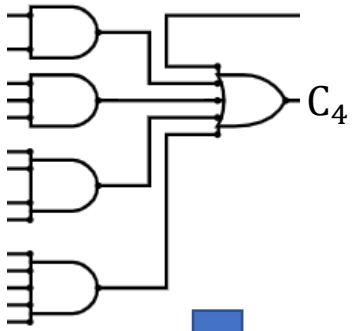


PG Logic: 4th Stage

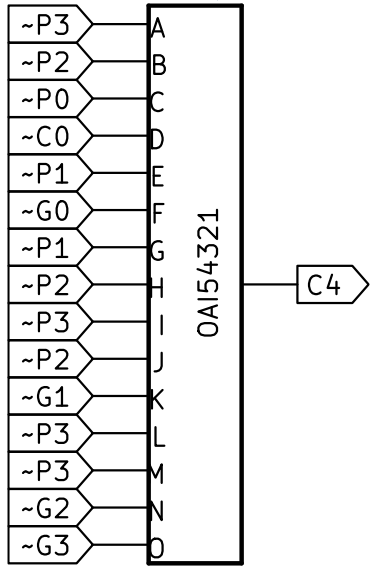
$$C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3$$
$$= \overline{G_3} \cdot (\overline{G_2} + \overline{P_3}) \cdot (\overline{G_1} + \overline{P_2} + \overline{P_3}) \cdot (\overline{G_0} + \overline{P_1} + \overline{P_2} + \overline{P_3}) \cdot (\overline{C_0} + \overline{P_0} + \overline{P_1} + \overline{P_2} + \overline{P_3})$$

↪ OAI54321



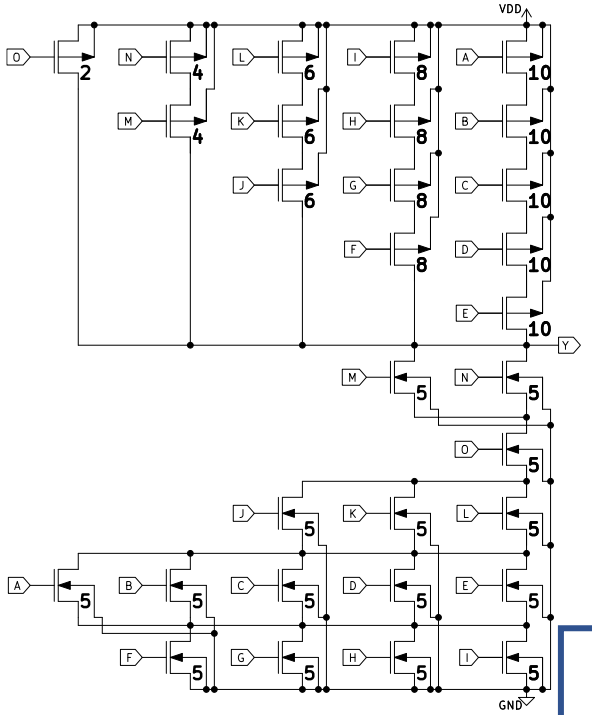


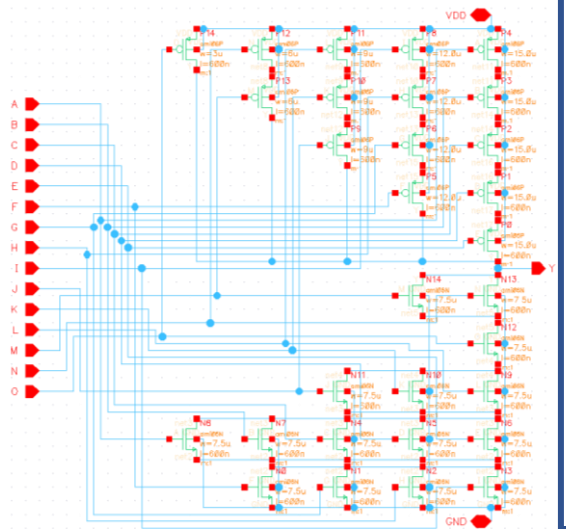
30T instead of 48T



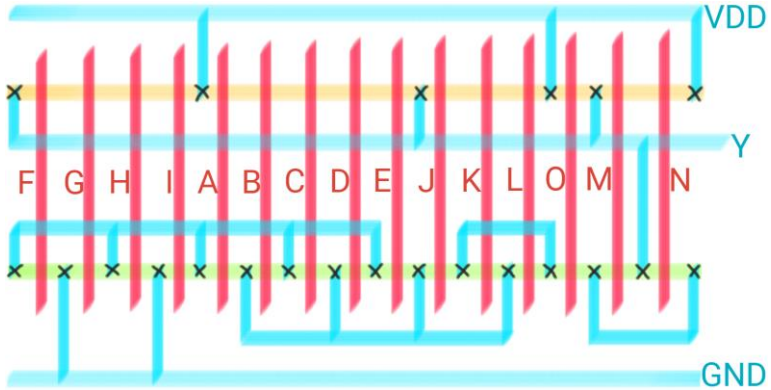
continued…

OAI54321 Schematic

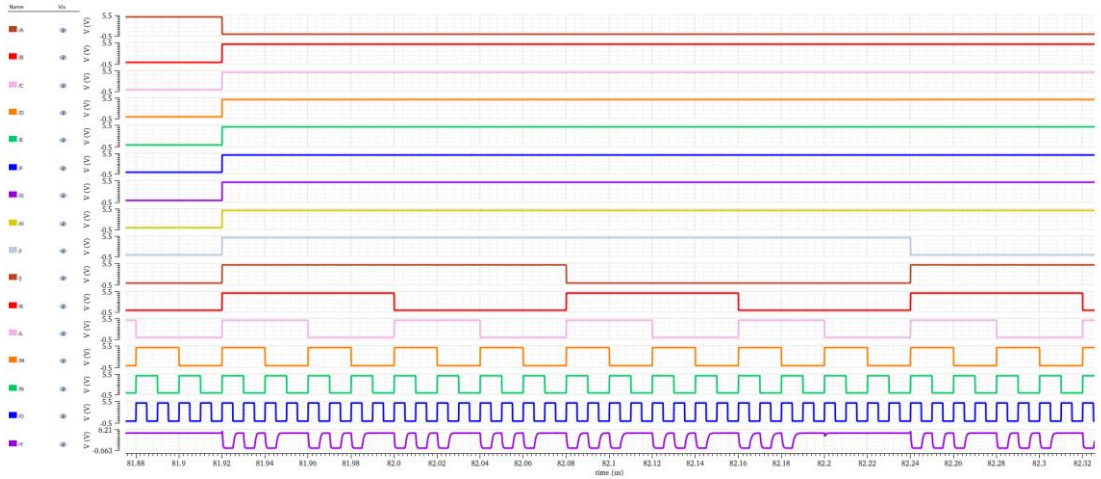




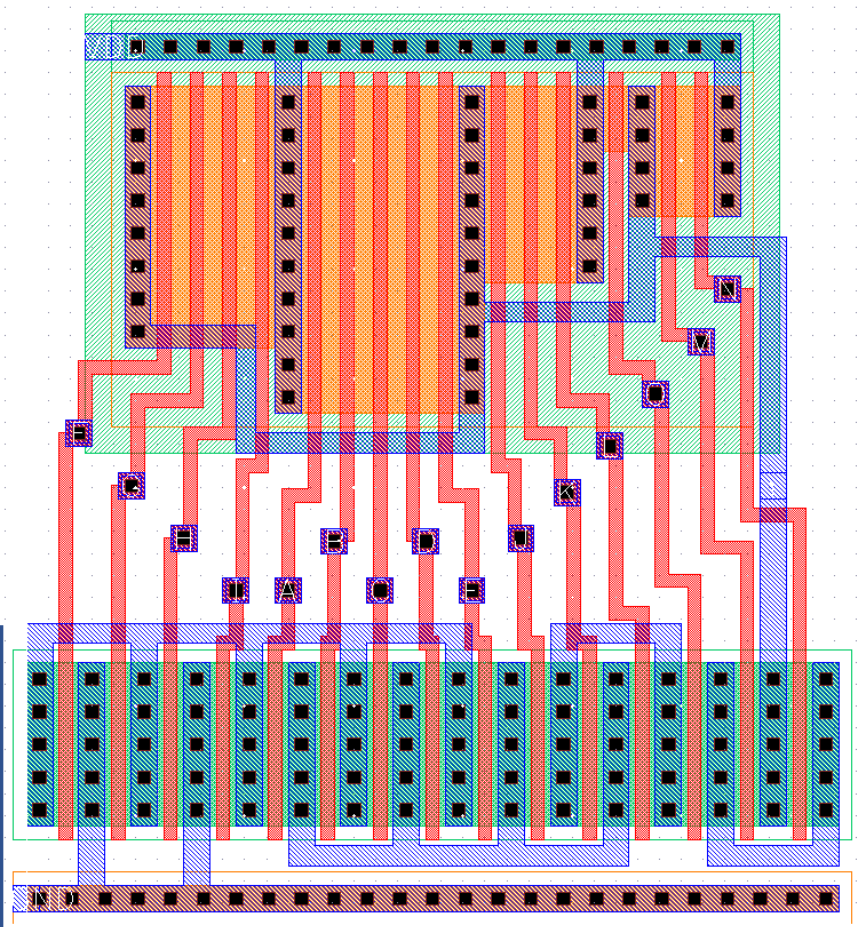
OAI54321 Stick Diagram



OAI54321 Transient Analysis (*cropped*)

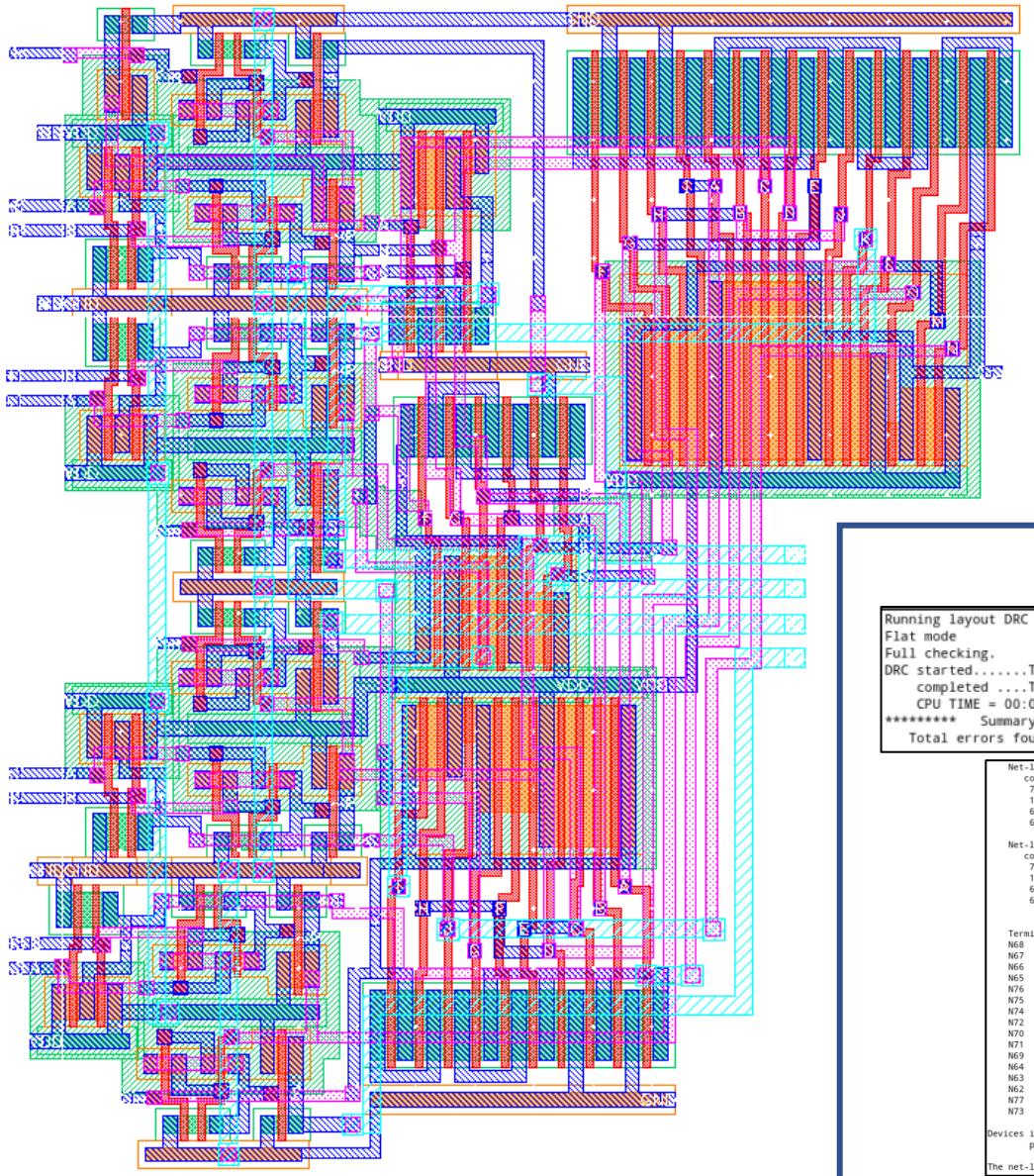


OAI54321 Layout



4-bit CLA unit

Layout

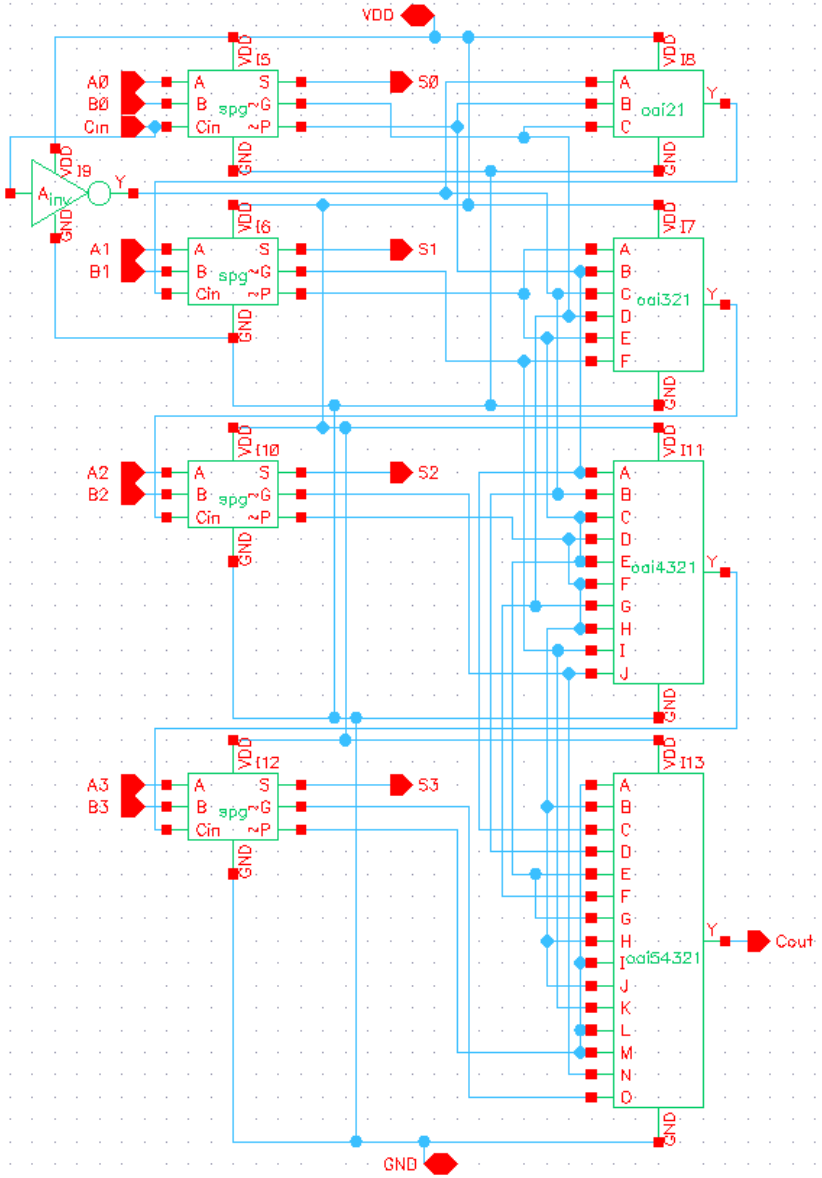


DRC & LVS

```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu Nov 17 22:34:07 2022
    completed ....Thu Nov 17 22:34:07 2022
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "fa_test layout"   *********
  Total errors found: 0
```

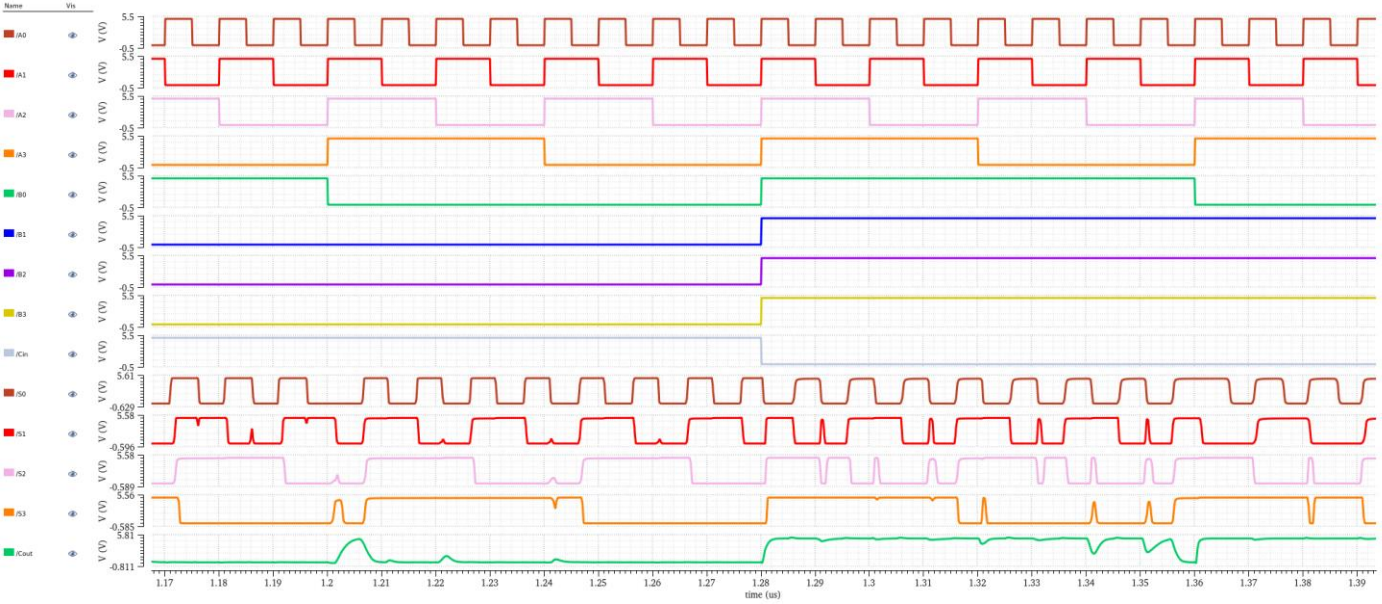
```
Net-list summary for /home/salam12/ece533/cadence/LVS/layout/netlist
   count
      78              nets
      16              terminals
      67              pmos
      67              nmos

Net-list summary for /home/salam12/ece533/cadence/LVS/schematic/netlist
   count
      78              nets
      16              terminals
      67              pmos
      67              nmos


Terminal correspondence points
N68       N3        A0
N67       N6        A1
N66       N11       A2
N65       N26       A3
N76       N2        B0
N75       N5        B1
N74       N24       B2
N72       N27       B3
N70       N4        Cin
N71       N15       Cout
N69       N1        GND
N64       N9        S0
N63       N10       S1
N62       N13       S2
N77       N25       S3
N73       N0        VDD

Devices in the netlist but not in the rules:
      pmos nmos

The net-lists match.
```

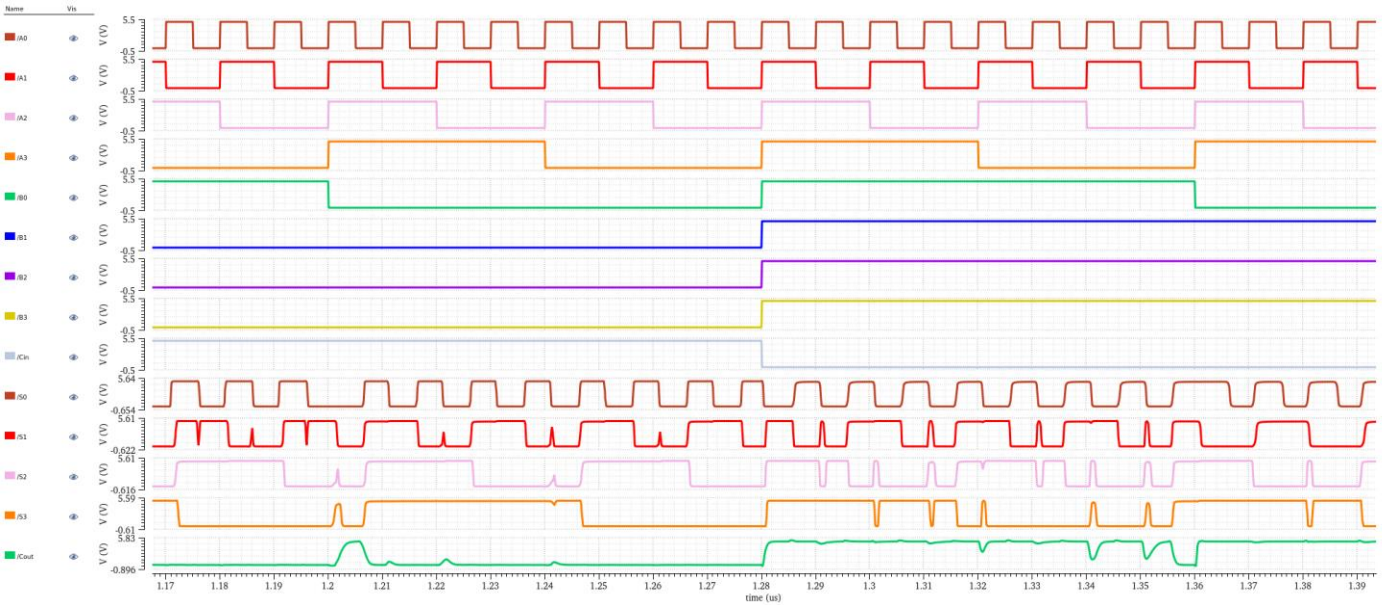
Schematic



continued…

CLA4 Transient Analysis (*cropped*)





Transistor Count			
Gate	**#Unit**	**FET/unit**	**Total FET**
SPG	4	16	64
INV	1	2	2
OAI21	1	6	6
OAI321	1	12	12
OAI4321	1	20	20
OAI54321	1	30	30
Aggregate Count			**134**

instead of **188**

Project Progress

Completed

- CLA4 unit
  - Layout & Schematic
    - NAND2
    - INV
    - XNOR2
    - OAIs

Remaining

- 4×4 Multiplier
  - #CLA4 unit needed → 5
  - #AND2 unit needed → 16
- 8-bit Adder
  - #CLA4 unit needed → 2
- Bank of D-Latches

Questions?
Concerns?
Comments?