

# Direct Memory Access Controller

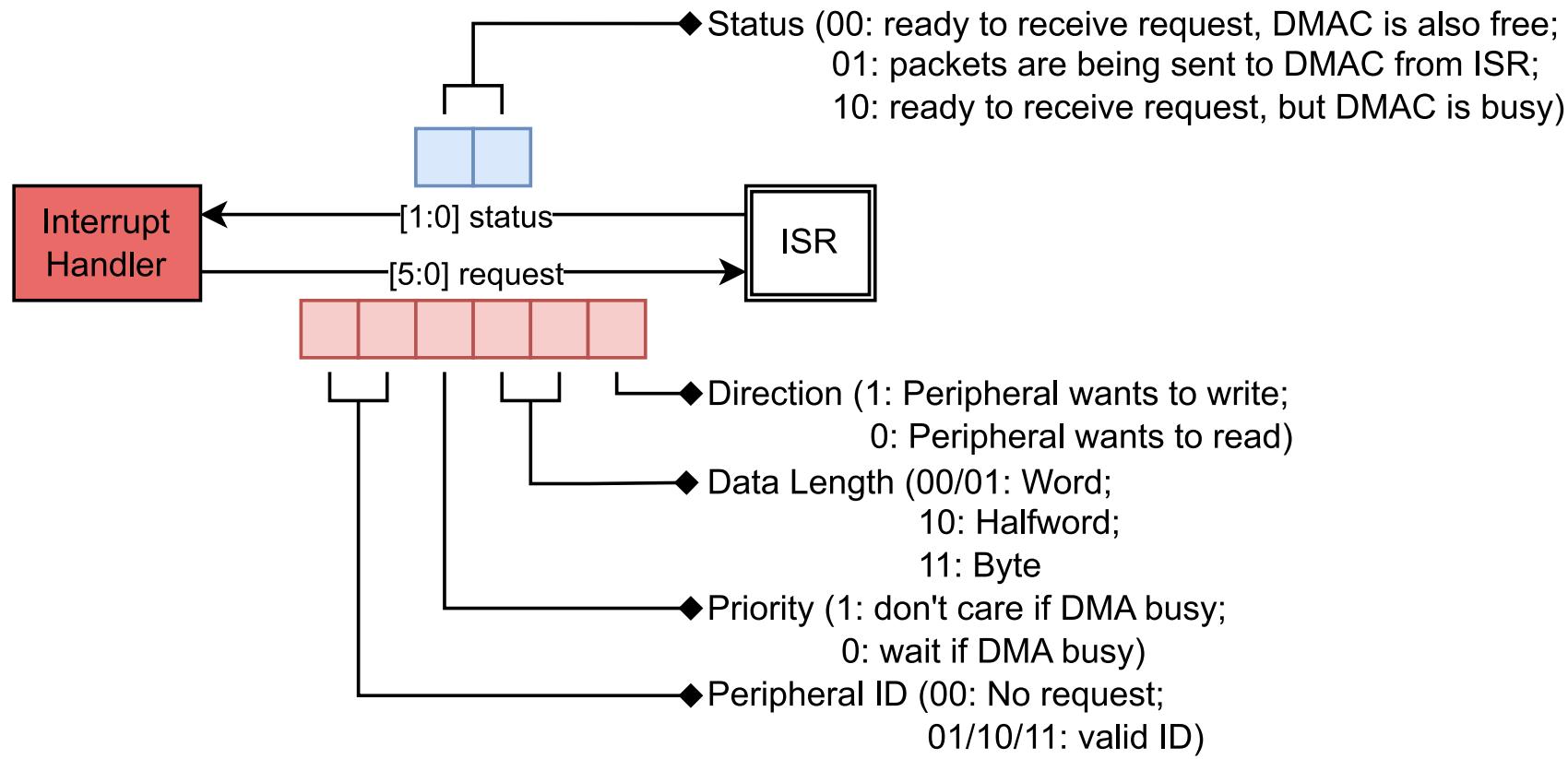
*Final Design Review*

ECE 551 – SoC Design

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- Tanjina Sabrin

# Interrupt Handler



# Interrupt Handler: Post-synthesis Simulation Result



1: Access required by peripheral 2, DMAC is not busy

2: Access granted to peripheral 2

3: ISR has sent the request to the DMAC and waiting for DMAC to start

4: DMAC is not busy, peripheral 2 and 3 requiring access

5: Access is granted to peripheral 2, due to its higher priority

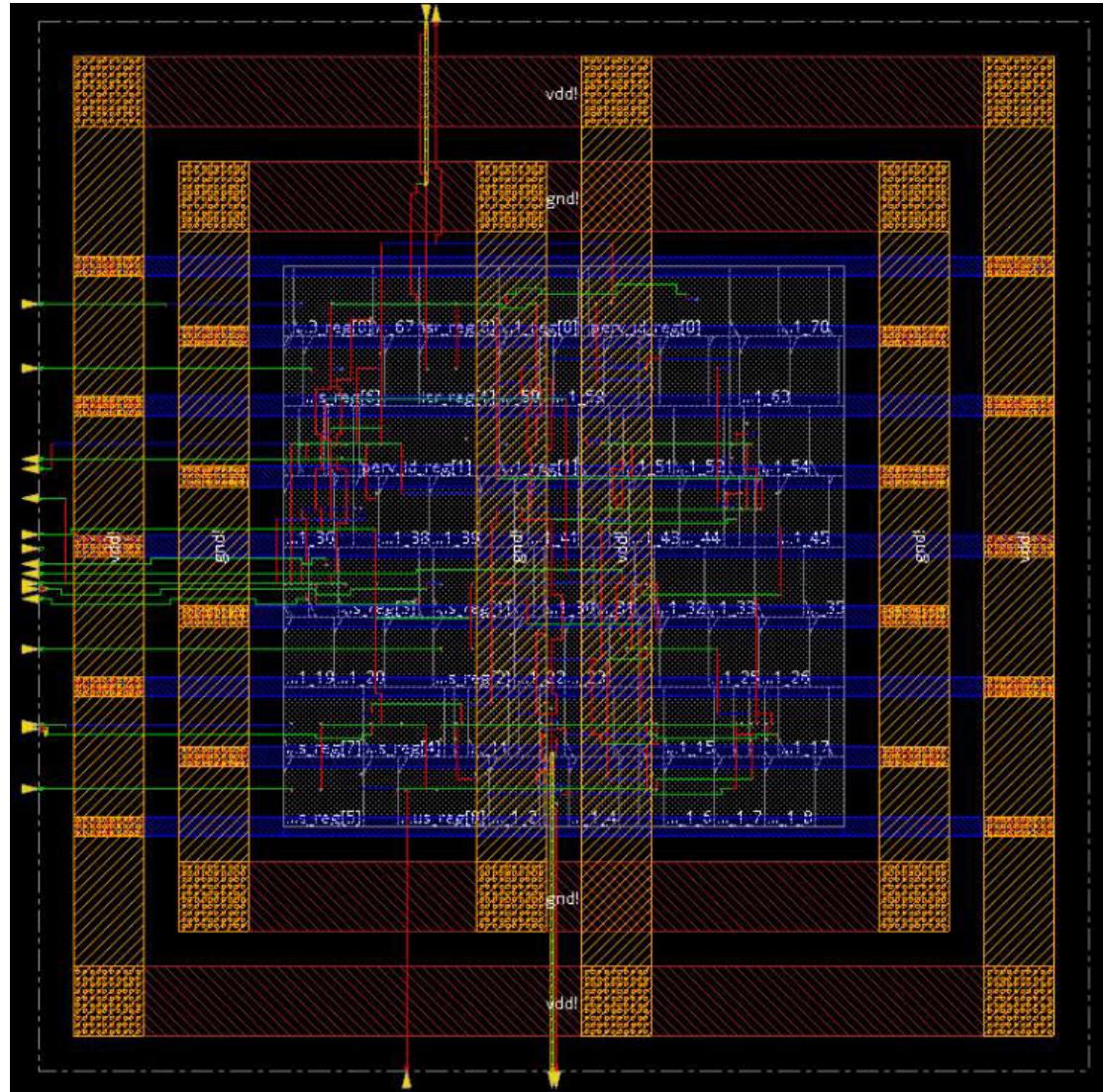
6: ISR has sent the request to the DMA and waiting for DMAC to start

7: DMAC is busy, but ISR can grant access to higher priority access requirement

8: Access required by peripheral 1

9: Access granted to peripheral 1, due to its higher priority

# Interrupt Handler: Layout and DRC Report



```
Terminal
File Edit View Search Terminal Help
#routeDesign: cpu time = 00:00:02, elapsed time = 00:00:02, memory = 931.88 (MB)
, peak = 963.59 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 1> #-check_implant false
# bool, default=true, user setting
#-check_ndr_spacing auto
# enums={true false auto}, default=auto
, user setting
#-report int_handler.drc.rpt
# string, default="", user setting
*** Starting Verify DRC (MEM: 1205.6) ***

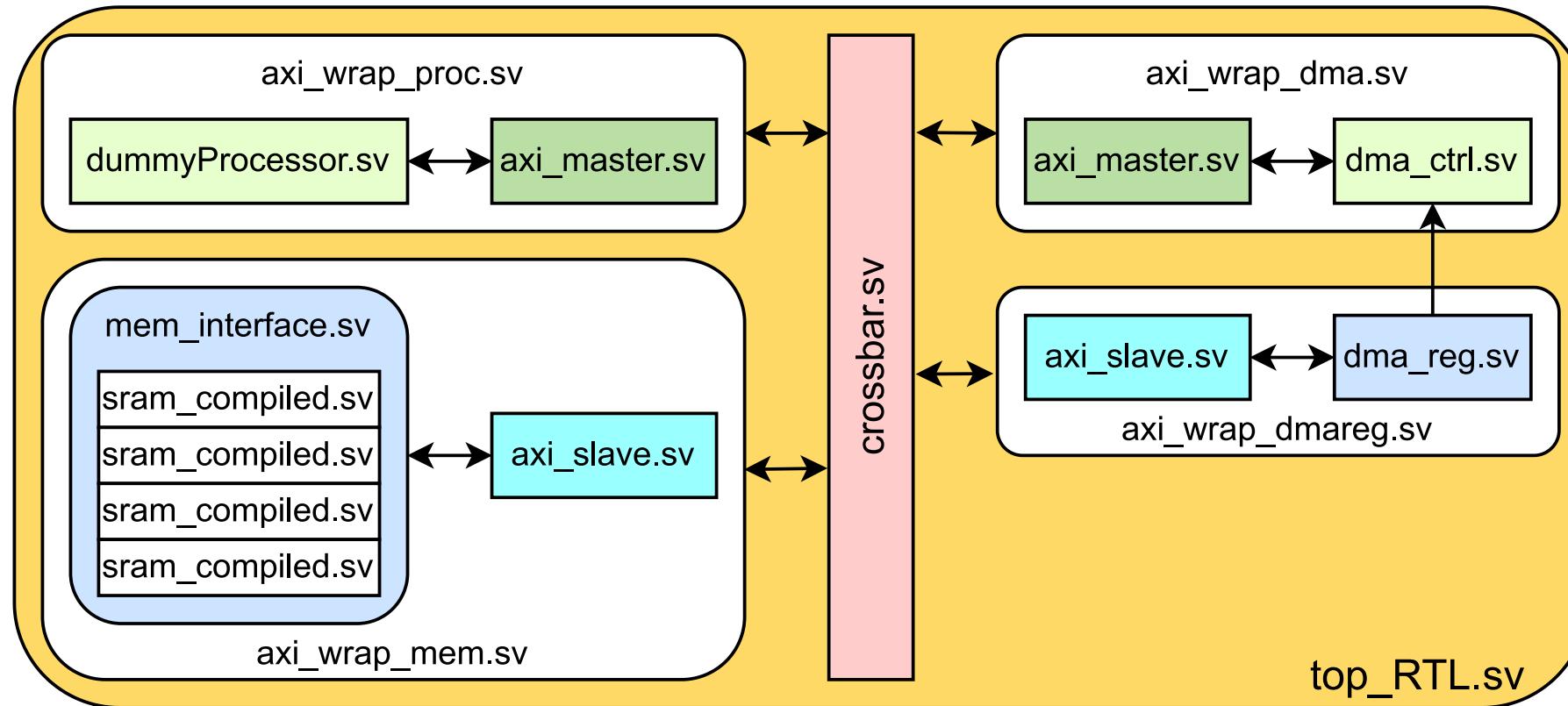
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 71.400 71.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

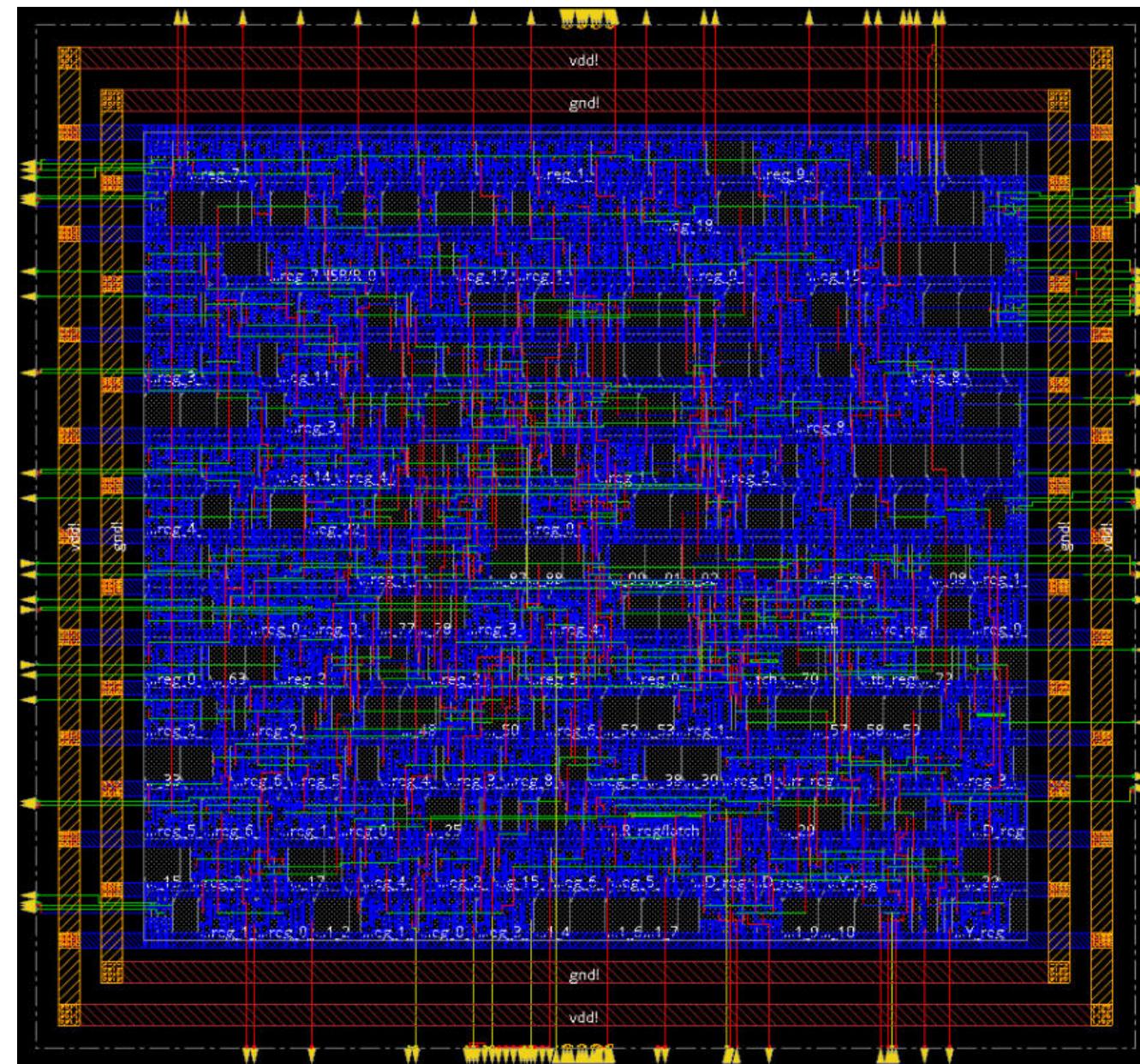
*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.0M) ***

innovus 1>
```

# Where we left: Overall Hierarchy



# ISR Wrapper



## *Includes*

- Interrupt Service Routine
- AXI\_master module

IV Geometry Violation: 0  
IV Connectivity Violation: 0

## IV DRC Report:

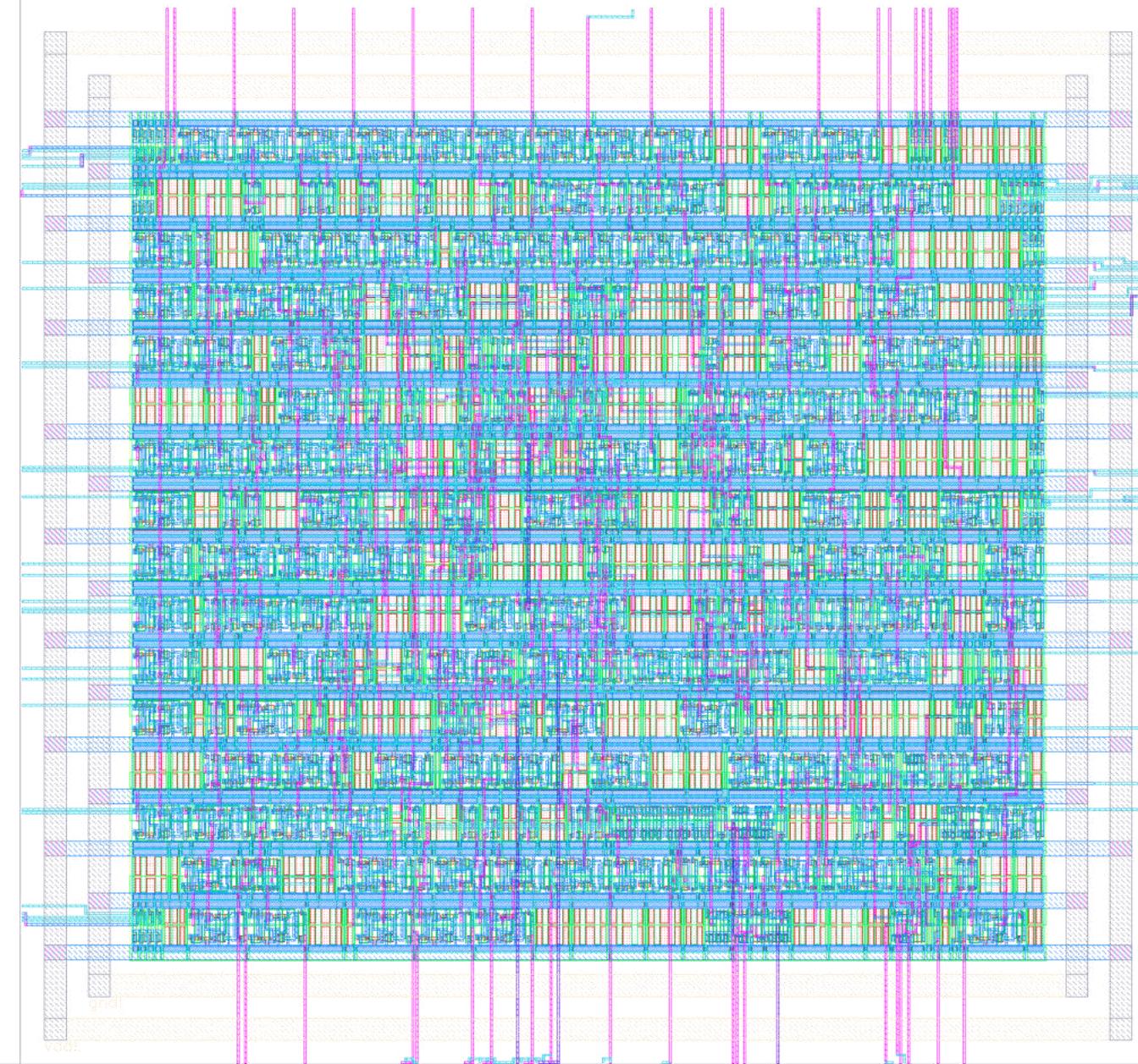
```
#-report axi_wrap_proc.drc.rpt          # string, default="", user sett
*** Starting Verify DRC (MEM: 2295.1) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198): The number of CPUs requested 8 is larger than the
mode, the number of CPUs verify_drc used is not larger than the number of
Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 103.700 96.560} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

continued...



## Calibre DRC Violations: 52

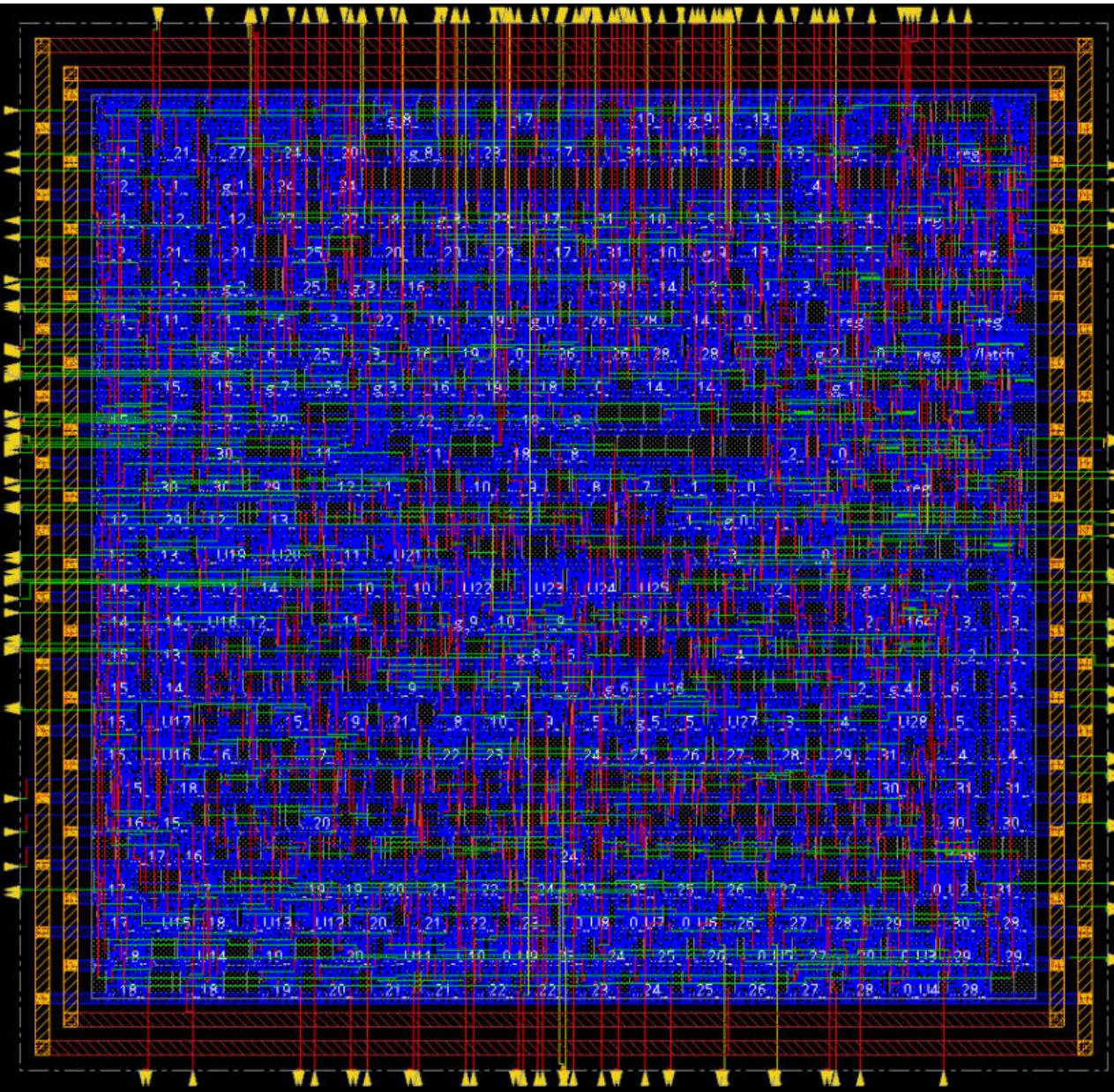
- (6) M3 vertex must not be connected to two short edges with length < 0.1
- (2) M2 vertex must not be connected to two short edges with length < 0.1
- (44) M3 minimum area >= 0.052

$$\text{Area} = (103.7 \times 96.56) \mu\text{m}^2 = 23037.9 \mu\text{m}^2$$

Density= 63.36%

\* Density denotes Chip Density (counting std cells and macros and IOs)

# DMAC Wrapper



## *Includes*

- DMA\_ctrl module
- AXI\_master module

IV Geometry Violation: 0

IV Connectivity Violation: 0

## IV DRC Report:

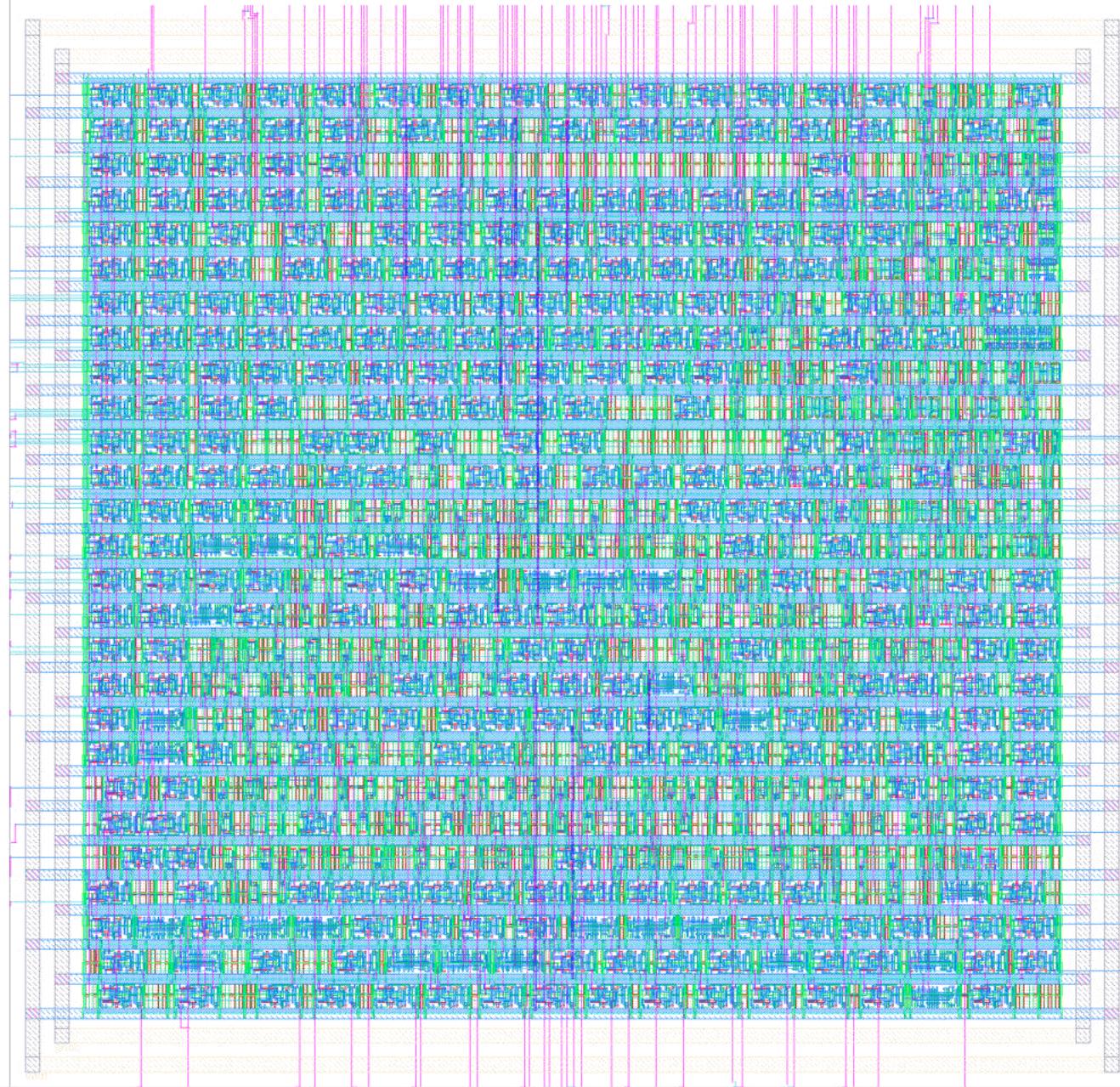
```
#-report axi_wrap_dma.drc.rpt      # string, default="", user setting
*** Starting Verify DRC (MEM: 2211.0) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198): The number of CPUs requested 8 is larger than that verify mode, the number of CPUs verify_drc used is not larger than the number of subareas. Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the verify mode is larger than the number of subareas.
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 77.760 148.920} 1 of 2 Thread : 0
VERIFY DRC ..... Thread : 1 finished.
VERIFY DRC ..... Sub-Area: {77.760 0.000 154.700 148.920} 2 of 2 Thread : 0
VERIFY DRC ..... Thread : 0 finished.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

*continued...*



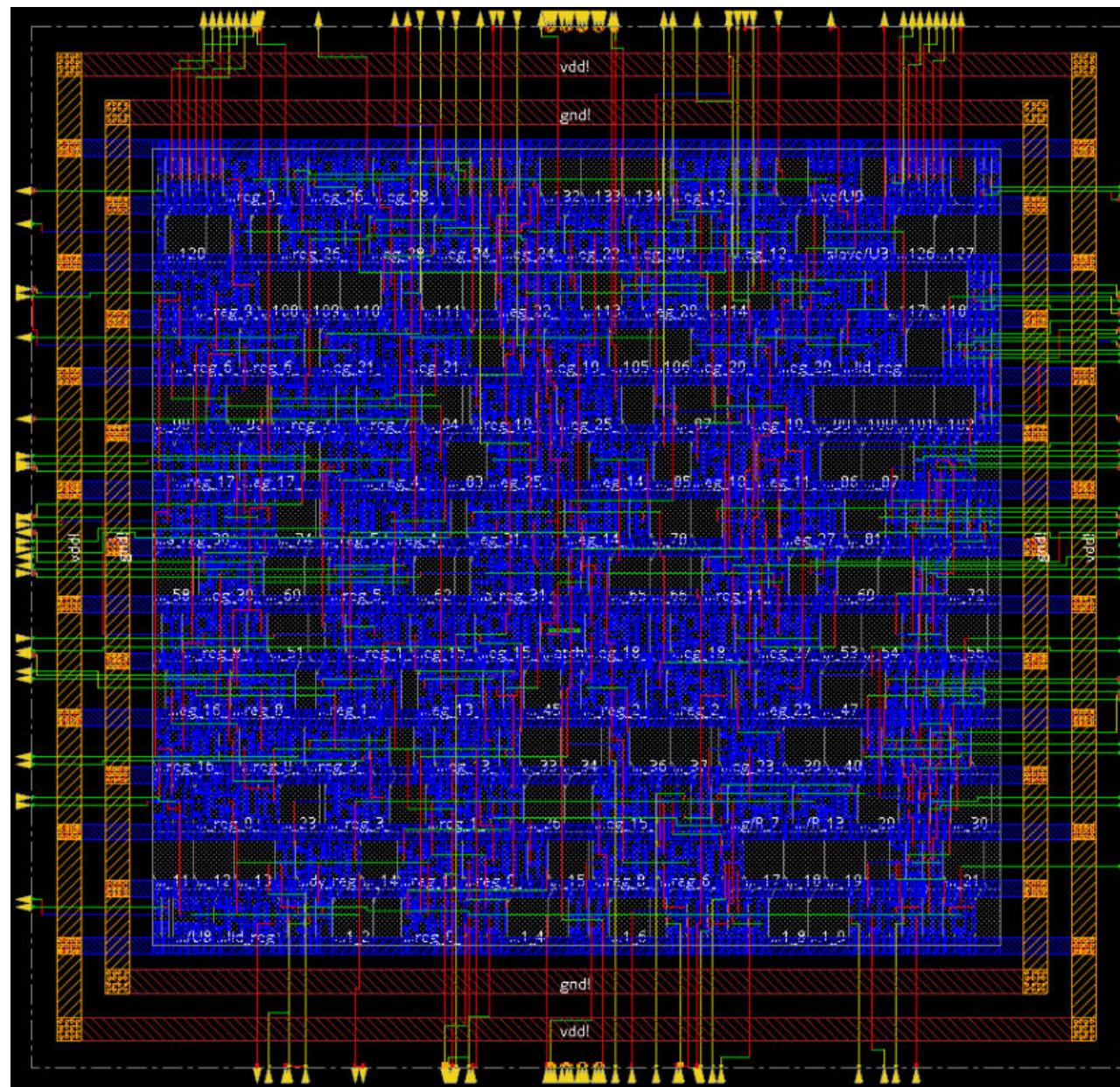
## Calibre DRC Violations: 58

- (18) M2 vertex must not be connected to two short edges with length < 0.1
- (40) M2 minimum area >= 0.052

$$\text{Area} = (154.7 \times 148.92) \mu\text{m}^2 = 23037.9 \mu\text{m}^2$$

Density = 74.92%

# DMA Register Wrapper



## *Includes*

- DMA\_reg module
- AXI\_slave module

## IV Geometry Violation: C

## IV Connectivity Violation: C

## **IV DRC Report:**

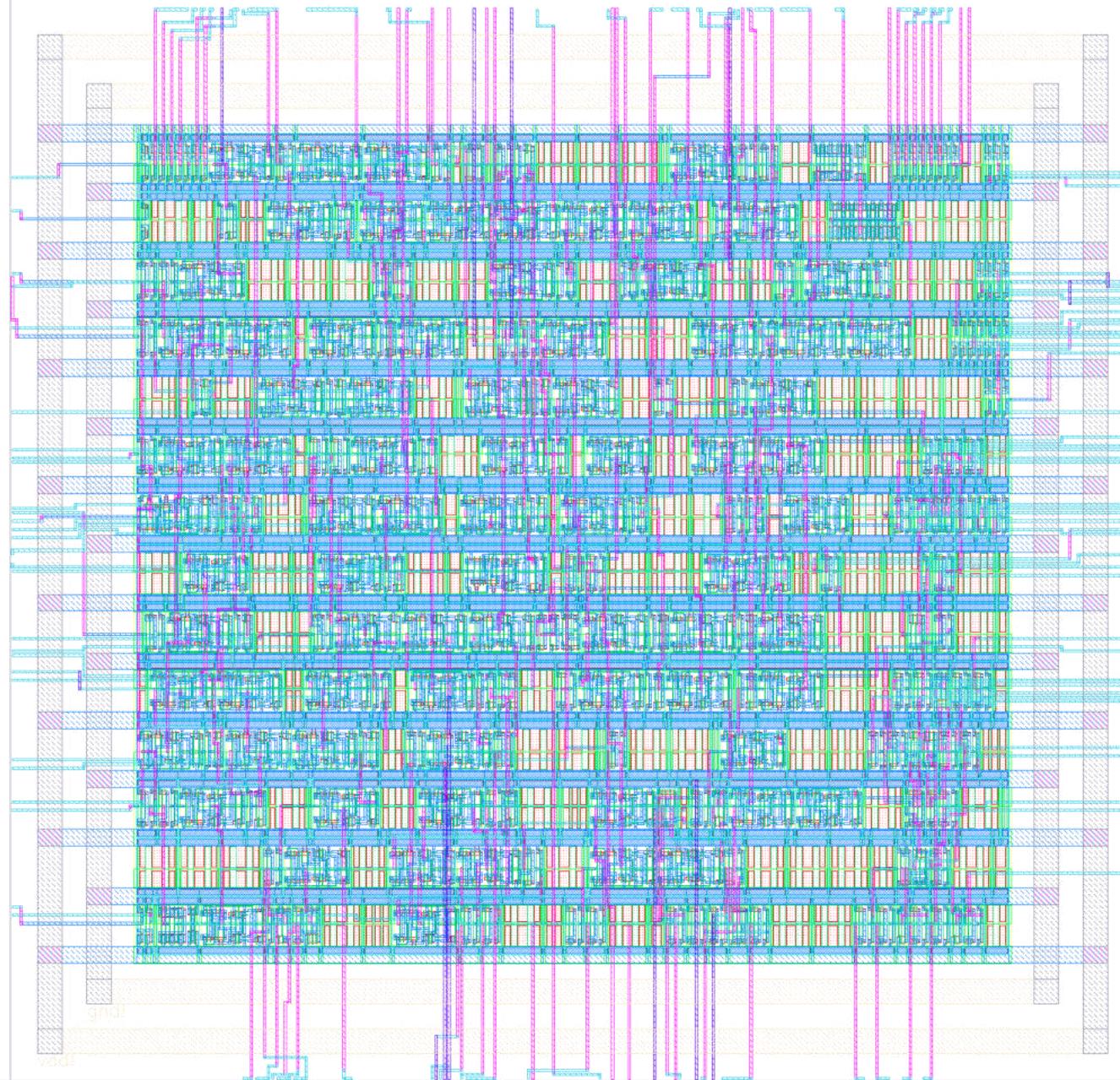
```
#-report axi_wrap_dmareg.drc.rpt      # string, default="", user set
*** Starting Verify DRC (MEM: 2233.0) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198): The number of CPUs requested 8 is larger than the
mode, the number of CPUs verify_drc used is not larger than the number of
Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 91.120 87.040} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

*continued...*



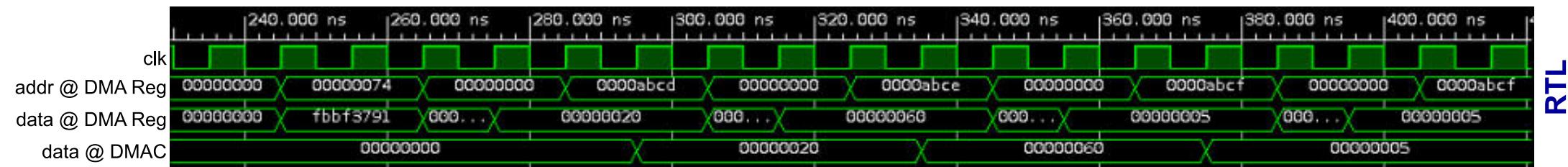
## Calibre DRC Violations: 29

- (2) M3 vertex must not be connected to two short edges with length < 0.1
- (27) M3 minimum area  $\geq 0.052$

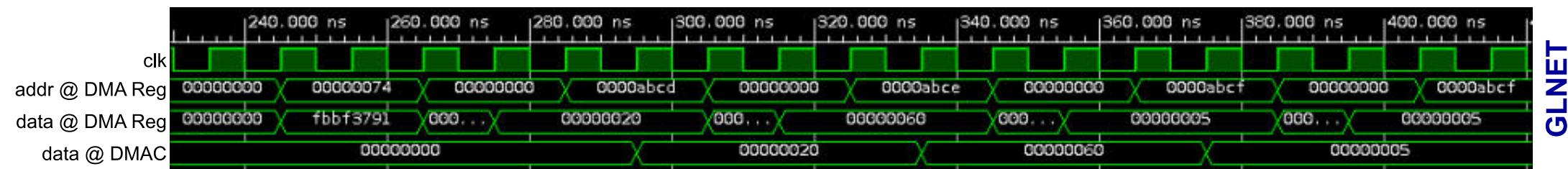
$$\text{Area} = (91.12 \times 87.04) \mu\text{m}^2 = 7931.1 \mu\text{m}^2$$

Density= 59.42%

*continued...*



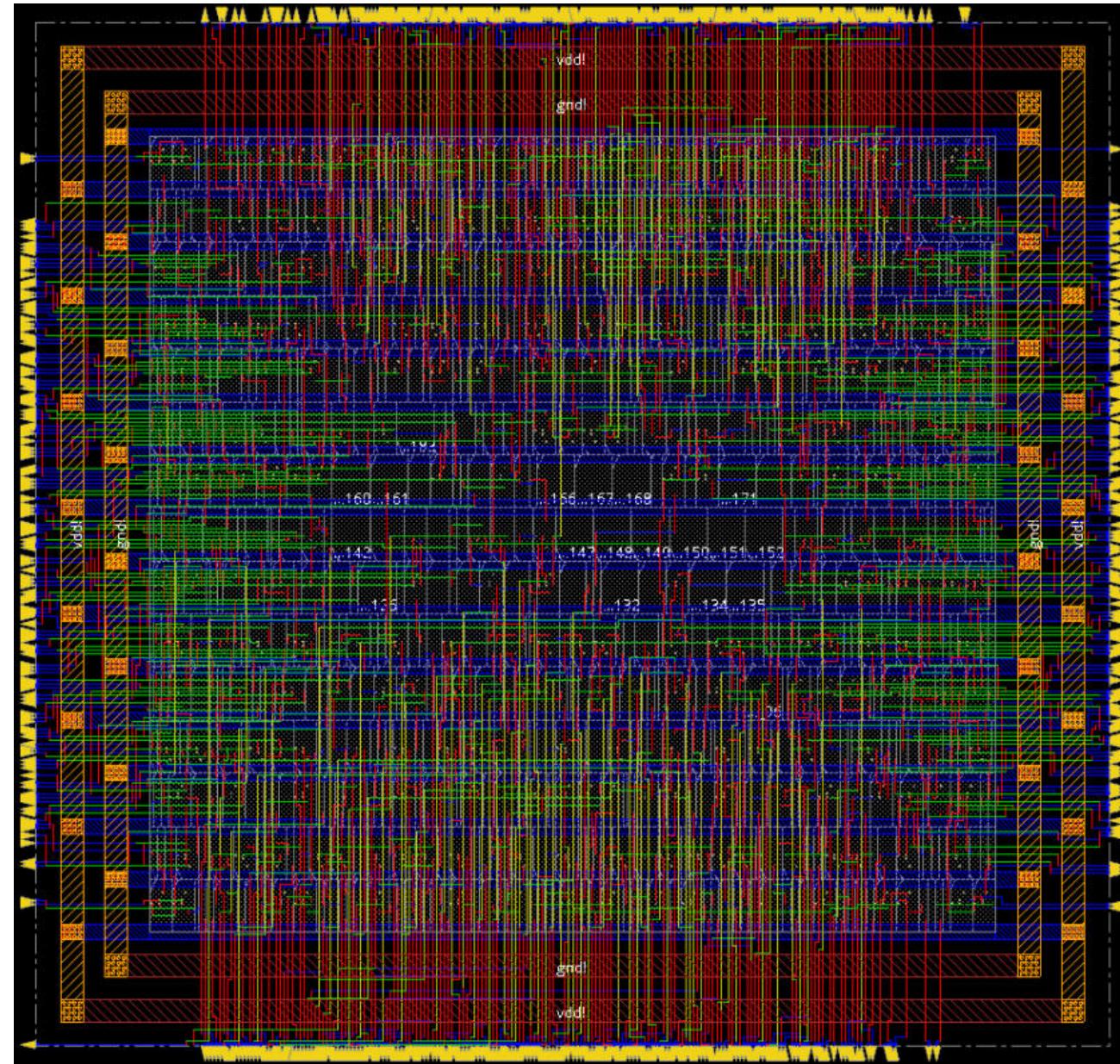
RTL



GLNET

DMA\_Reg and DMAC gate-level netlist verification

# Crossbar



## *Full matrix cross-connection*

IV Geometry Violation: 0  
IV Connectivity Violation: 0

## IV DRC Report:

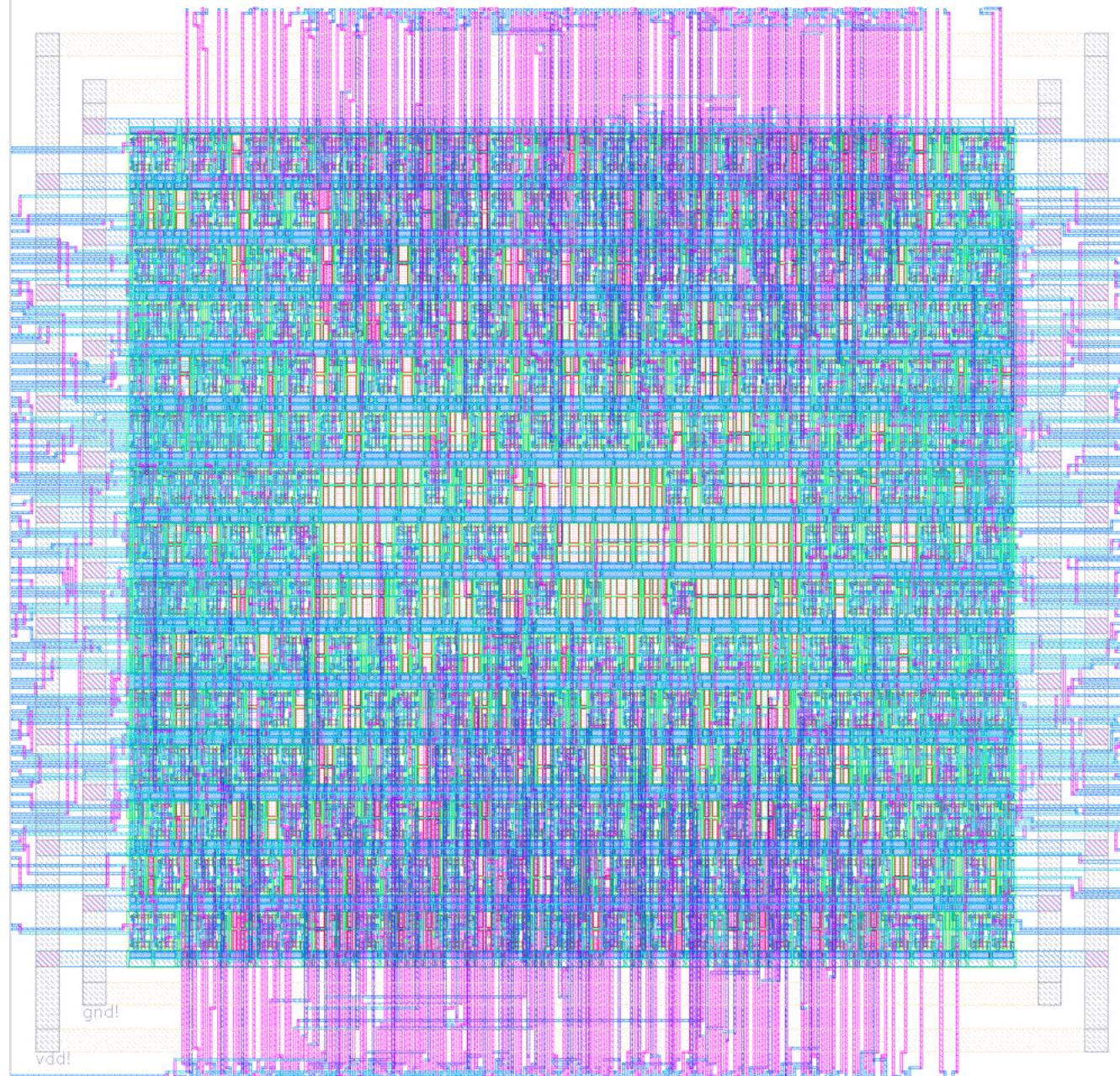
```
#-report crossbar.drc.rpt          # string, default="", user sett
*** Starting Verify DRC (MEM: 1055.4) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 96.220 91.800} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

continued...



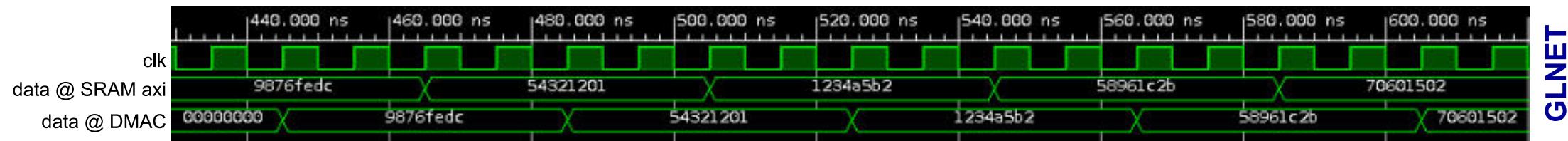
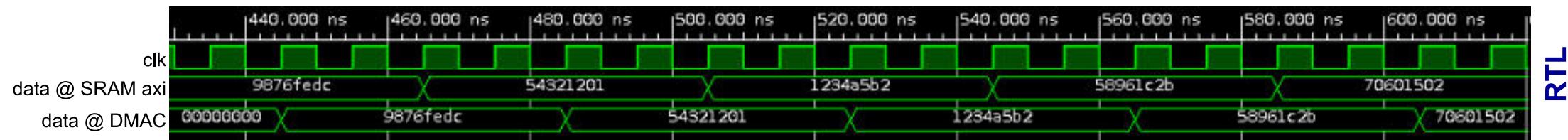
Calibre DRC Violations: 52

- (52) M1 minimum area  $\geq 0.042$

$$\text{Area} = (96.22 \times 91.8) \mu\text{m}^2 = 8832.99 \mu\text{m}^2$$

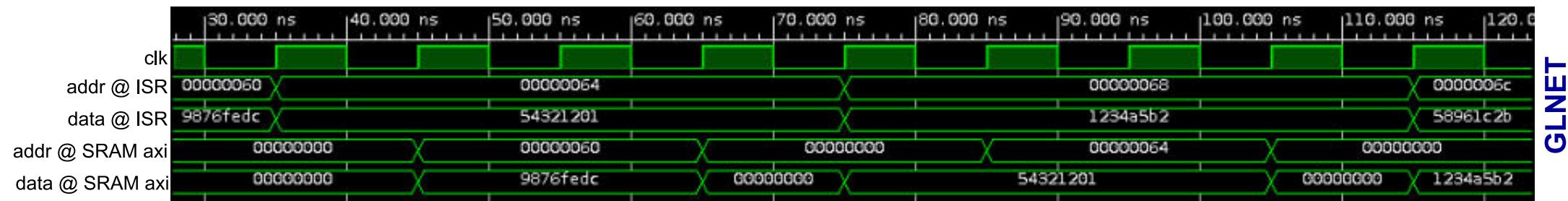
Density= 61.29%

*continued...*



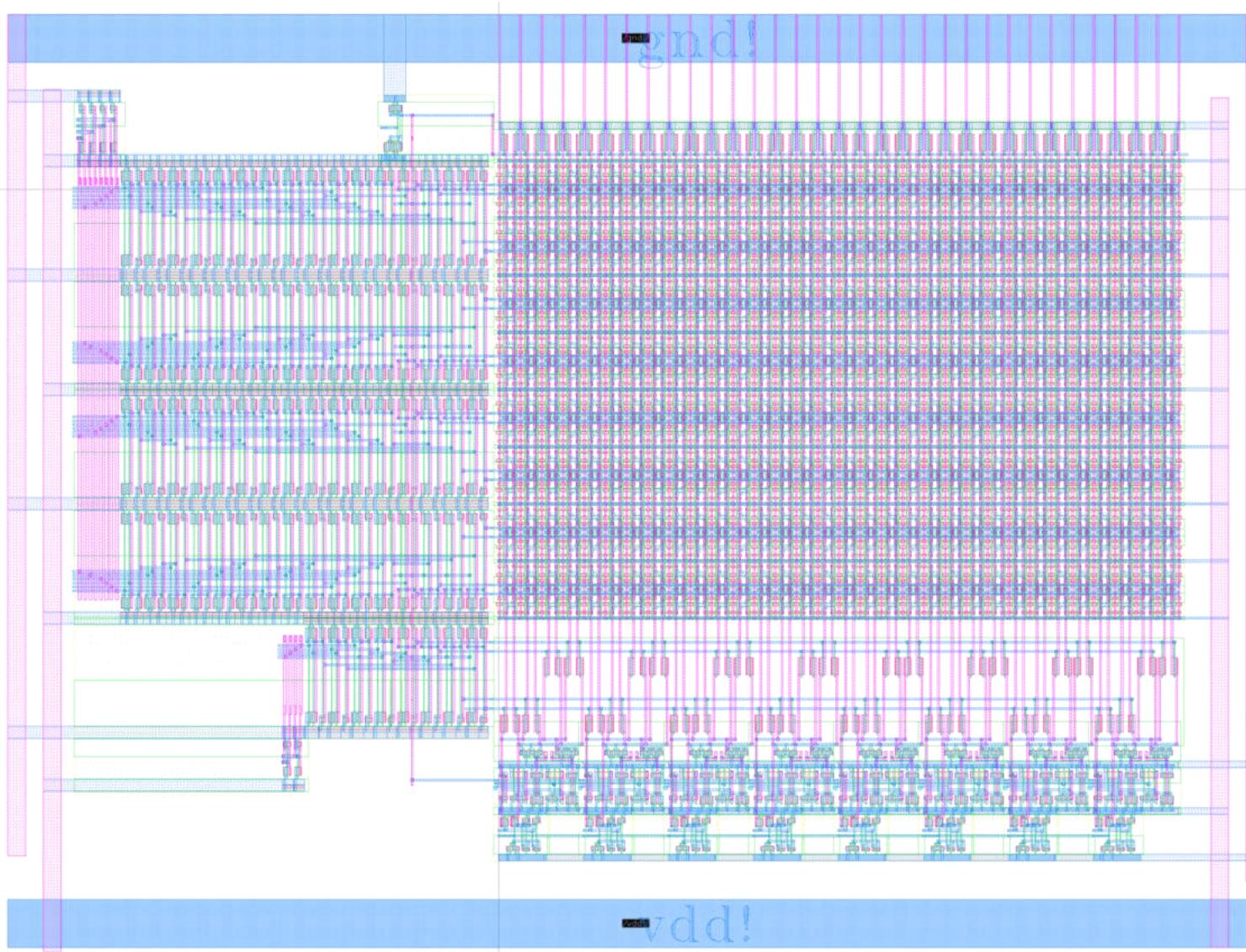
**crossbar** gate-level netlist verification

*continued...*



**axi\_master** and **axi\_slave** gate-level netlist verification

# Compiled SRAM Array

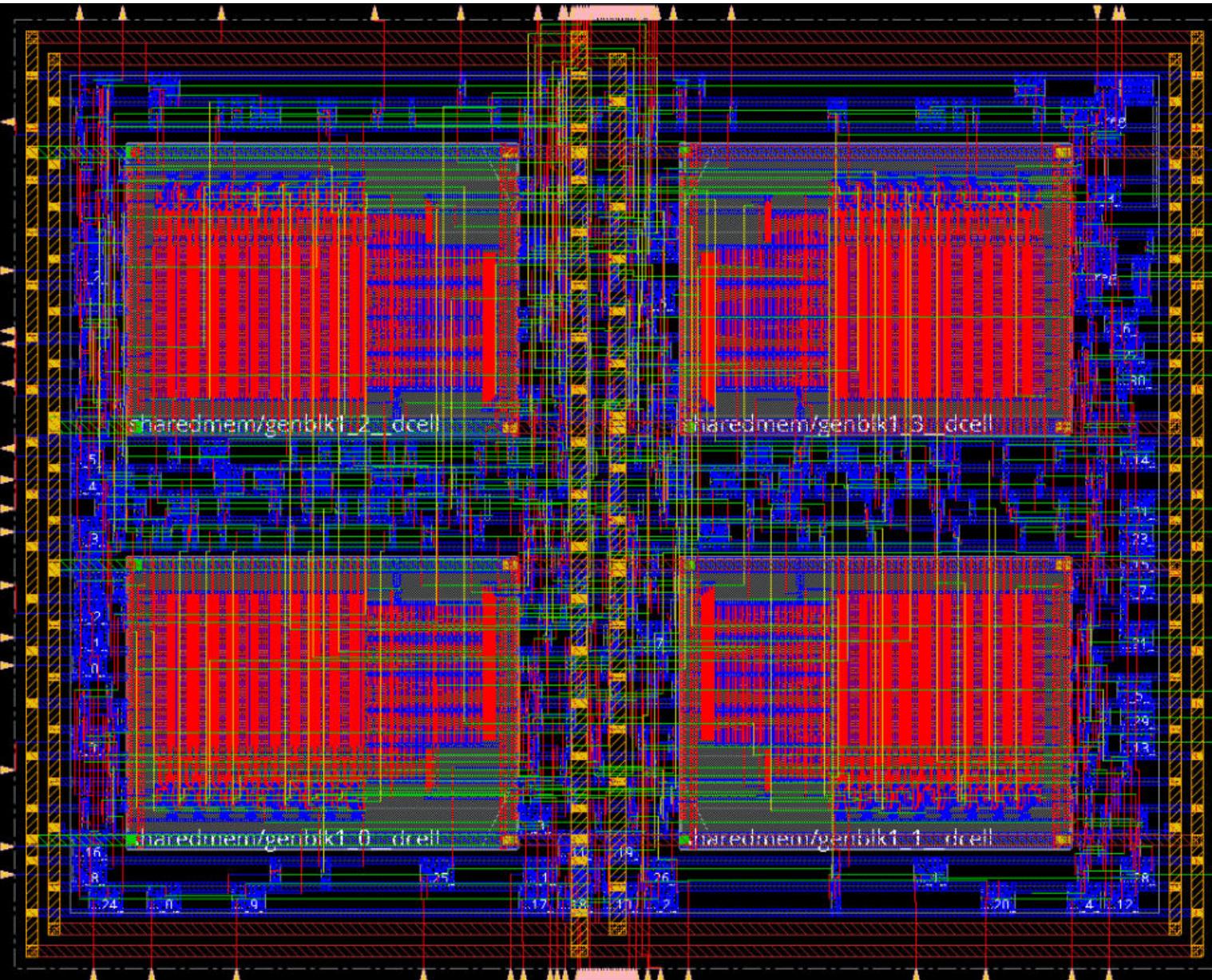


Topology: 16×32×8

Calibre DRC Violation: 0

Area=  $(70.99 \times 52.98)\mu m^2 = 3761.05 \mu m^2$

# Memory Wrapper



## *Includes*

- 4 banks of SRAM
- Memory controller
- AXI\_slave module

## IV DRC Report:

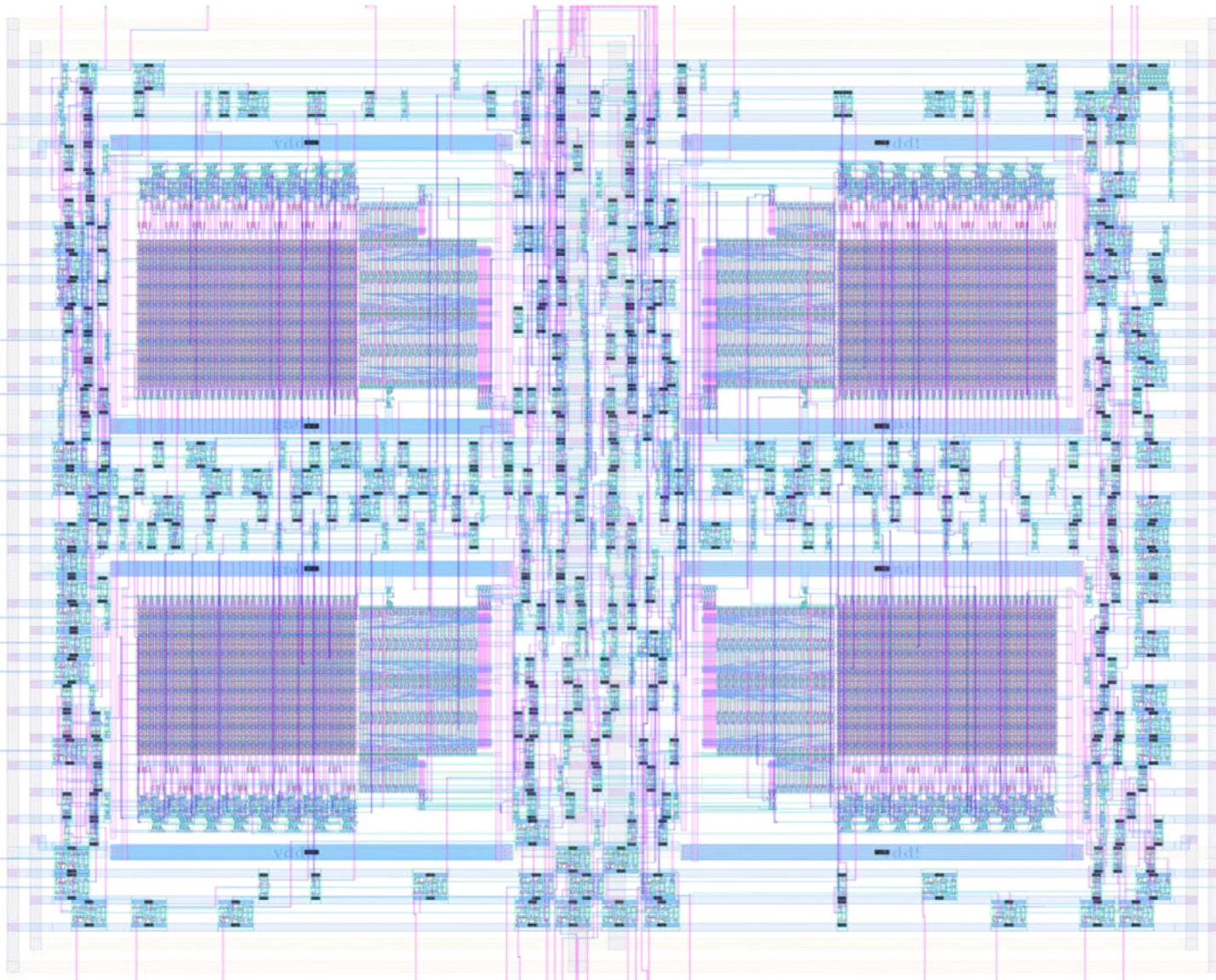
```
#-report axi_wrap_mem.drc.rpt      # string, default="", user setting
*** Starting Verify DRC (MEM: 1047.2) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 109.440 86.400} 1 of 4
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {109.440 0.000 218.280 86.400} 2 of 4
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 86.400 109.440 172.720} 3 of 4
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {109.440 86.400 218.280 172.720} 4 of 4
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.2 ELAPSED TIME: 0.00 MEM: 7.0M) ***
```

continued...



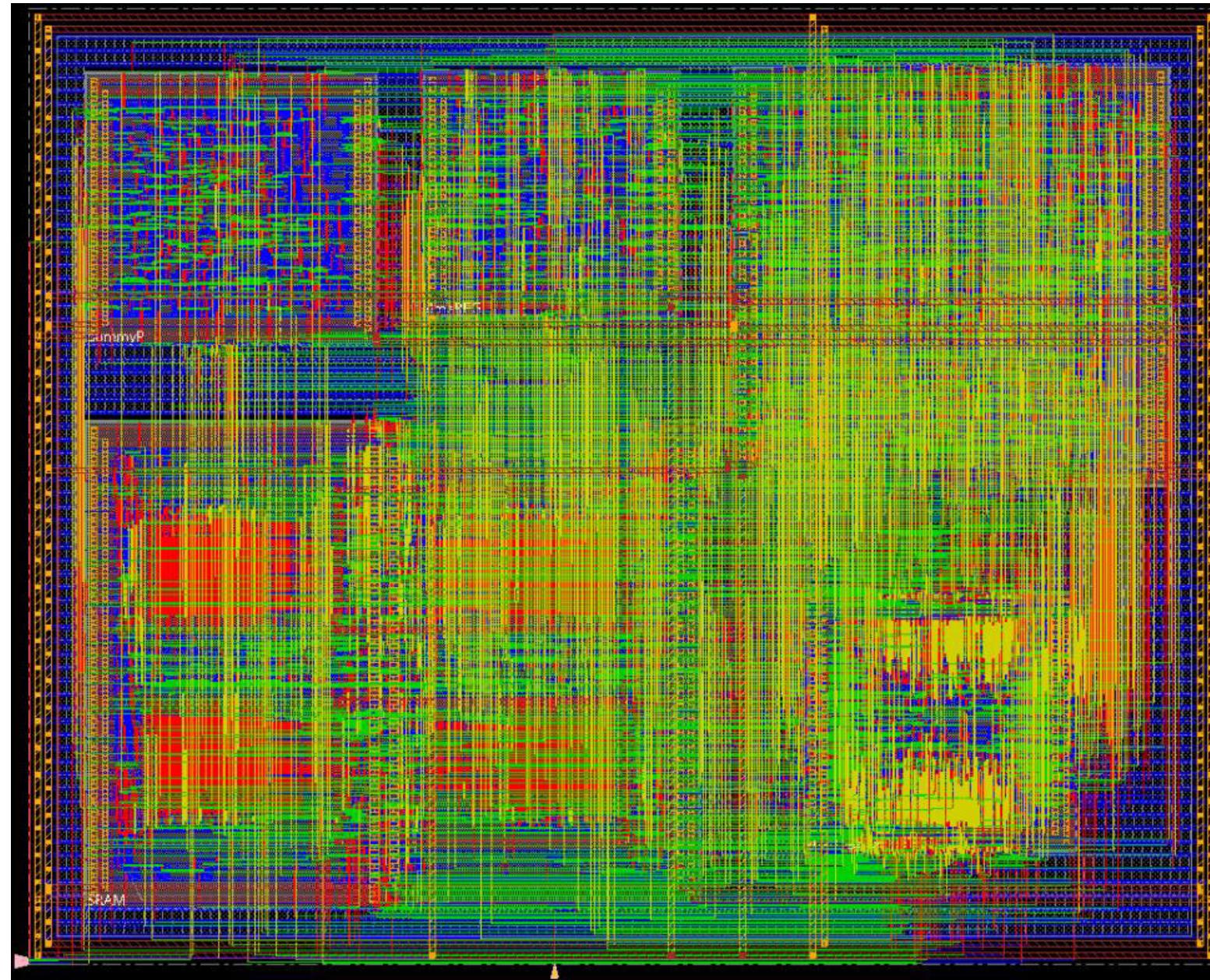
## Calibre DRC Violations: 169

- (15) BF minimum space and notch > = 0.47
- (40) RX minimum width > = 0.08
- (40) RX minimum space and notch > = 0.11
- (4) M3 vertex must not be connected to two short edges with length < 0.1
- (12) M1 vertex must not be connected to two short edges with length < 0.09
- (6) M1 minimum space and notch > = 0.09
- (2) (V3 Array with width > 1.090 ) minimum space V3 array >= 0.700
- (21) M2 minimum area >= 0.052
- (15) NW minimum space > = 0.47
- (3) M2 minimum space to ( M2 WITH WIDTH > 0.200), for run length > 0.380, >= 0.12
- (11) M2 minimum space to ( M2 WITH WIDTH > 0.420), for run length > 0.420, >= 0.16

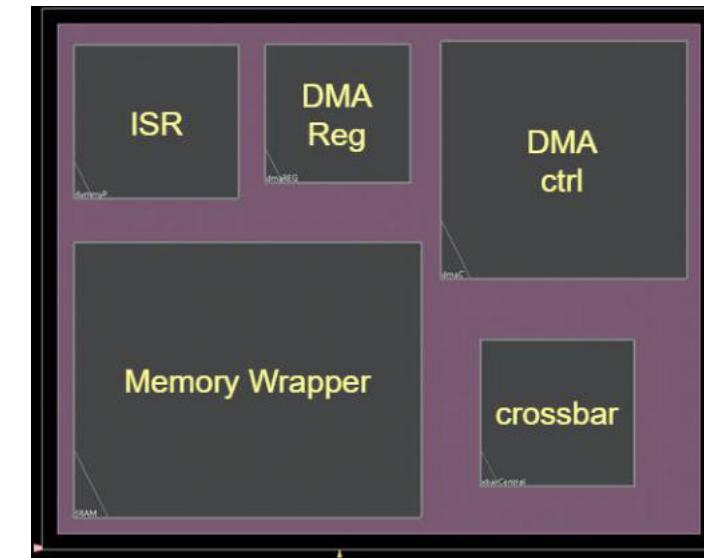
$$\text{Area} = (218.28 \times 172.72) \mu\text{m}^2 = 37701.32 \mu\text{m}^2$$

Density = 52.13%

# Top Module



## Amoeba View:



## IV DRC Report:

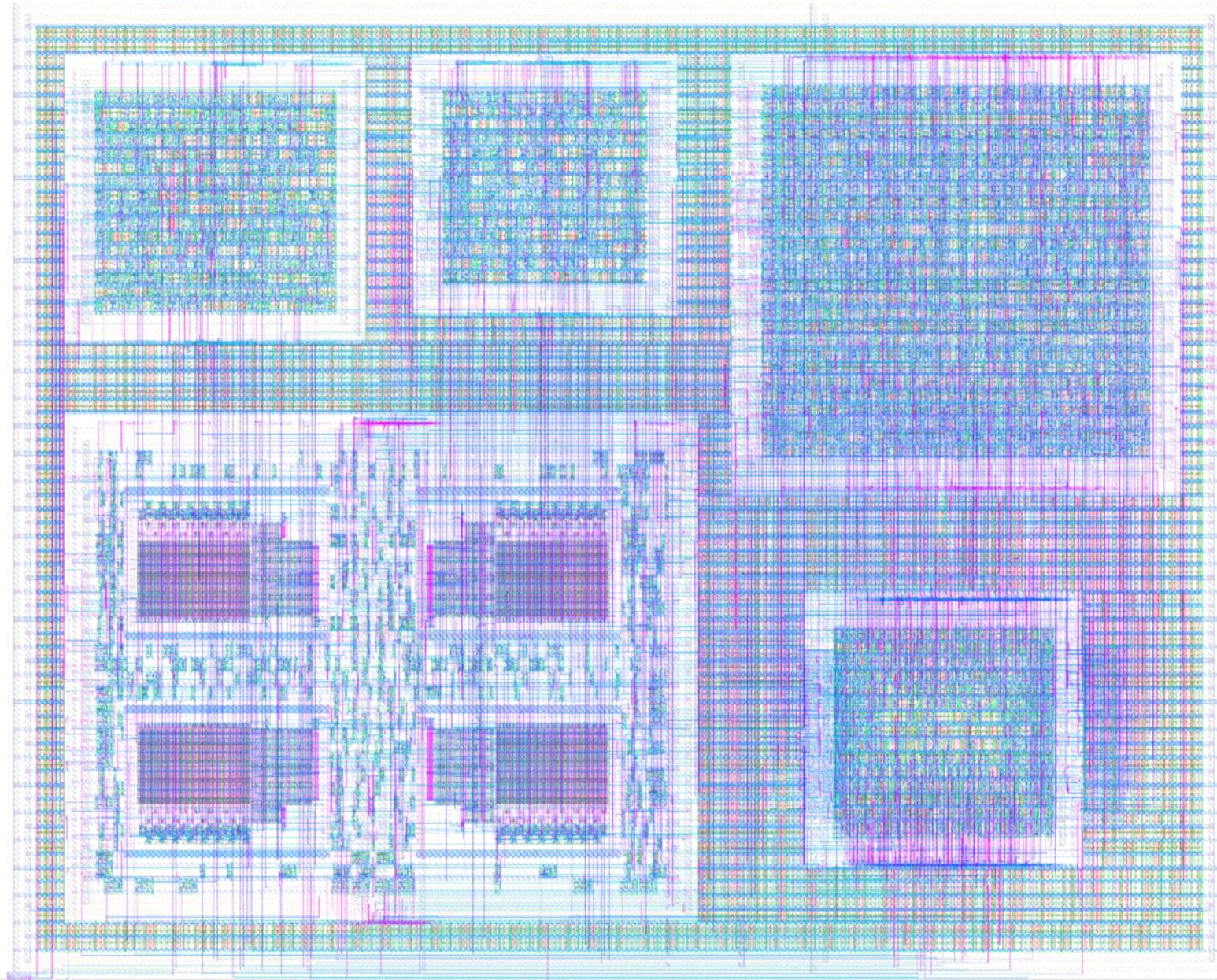
```
#-report top_RTL.drc.rpt          # string, default="", user setting
*** Starting Verify DRC (MEM: 2160.8) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 227.520 141.120 339.320} 7 of 9 Thread : 0
VERIFY DRC ..... Sub-Area: {282.240 0.000 422.620 113.760} 3 of 9 Thread : 7
VERIFY DRC ..... Sub-Area: {282.240 227.520 422.620 339.320} 9 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {0.000 0.000 141.120 113.760} 1 of 9 Thread : 3
VERIFY DRC ..... Sub-Area: {0.000 113.760 141.120 227.520} 4 of 9 Thread : 3
VERIFY DRC ..... Sub-Area: {282.240 113.760 422.620 227.520} 6 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {141.120 0.000 282.240 113.760} 2 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {141.120 227.520 282.240 339.320} 8 of 9 Thread : 3
VERIFY DRC ..... Thread : 4 finished.
VERIFY DRC ..... Thread : 7 finished.
VERIFY DRC ..... Sub-Area: {141.120 113.760 282.240 227.520} 5 of 9 Thread : 3
VERIFY DRC ..... Thread : 3 finished.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.4  ELAPSED TIME: 0.00  MEM: 32.0M) ***
```

*continued...*



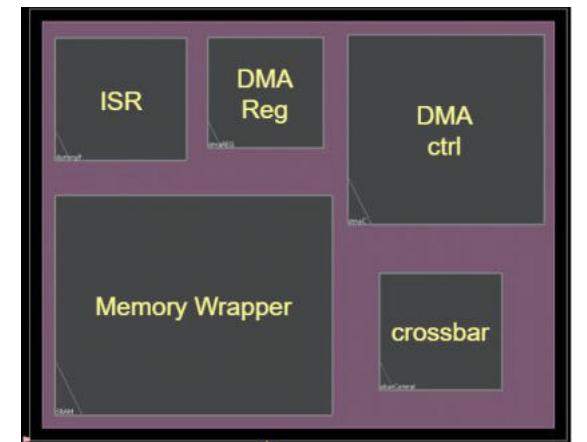
## Calibre DRC Violations: 1235

- (362) M1 minimum space and notch  $\geq 0.09$
- (141) M3 minimum space and notch  $\geq 0.1$
- (131) M2 minimum space and notch  $\geq 0.1$
- (111) M2 vertex must not be connected to two short edges with length  $< 0.1$
- (60) M3 vertex must not be connected to two short edges with length  $< 0.1$
- and some more

---

$$\text{Area} = (422.62 \times 339.32) \mu\text{m}^2 = 143403.42 \mu\text{m}^2$$

Density = 87.73%



**Questions?  
Comments?  
Concerns?**